Global Journal of Engineering and Technology Advances
eISSN: 2582-5003
Cross Ref DOI: 10.30574/gjeta
Journal homepage: https://gjeta.com/

(RESEARCH ARTICLE)

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Grid interface of solar PV transformer-less inverters using enhanced phase locked loop

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Global Journal of Engineering and Technology Advances, 2022, 11(03), 052–058

Publication history: Received on 13 May 2022; revised on 18 June 2022; accepted on 20 June 2022

Article DOI: https://doi.org/10.30574/gjeta.2022.11.3.0095

Abstract

The era of Renewable Energy sources has overtaken the usage of conventional energy sources like coal, fossil fuels etc. This paper presents grid interface of single phase transformerless inverter system using enhanced phase locked loop. To connect solar PV with grid it is required to estimate phase angle, voltage amplitude and phase angle measurement of grid and the output of inverter. It is required to track exact utility voltage vector for reliable control of power to the grid. This paper compares the frequency measurement and phase angle and voltage amplitude using simple phase locked loop system along with enhanced phase locked loop so that the enhanced phase locked loop (EPLL) is proved to be giving superior performance over simple phase locked loop. The simulation of both the techniques are pursued and the results are compared.

Keywords: Phase angle Measurement; Enhanced Phase locked Loop; Transformerless inverter; Solar PV transformer

1. Introduction

The fact that the conventional sources are not adequate for the coming years so that it makes an inevitable attempt to increase the percentage of renewable energy sources to be used. In this scenario the solar PV found to be most used renewable energy sources, due to its simplified conversion technology [1]. As the renewable energy sources like solar Photo voltaic (PV) generates DC, an Inverter is required to convert into AC and to supply it to grid. The converter can be DC-DC, to maintain the DC voltage constant at the DC link capacitor of the input of the inverter. Various converters can be used at various stages of power conversion. The converter can be a DC-AC which feeds the power from solar to grid. A high frequency transformer is used in case of DC-DC converters, on DC side otherwise a low frequency transformer in case of Inverter on AC side. In either of the cases the transformer is used which will be inherent part of the converter thus occupying space, increases the cost of the system and reduces the efficiency of the system. Thus, to reduce the cost and space occupied by the system the transformerless inverters are into practice [2]. The power electronics converters are used in the conversion of renewable energy sources from dc-dc and dc-ac Solar PV inverters need either a high frequency transformer on dc side shown in Figure.1. or a low frequency transformer on ac side to provide galvanic isolation as shown in Figure2. But by avoiding transformer as shown in Figure. 3..efficiency of the conversion can be improved, and size of the inverter can also be reduced considerably. In view of this advantages, research on transformer less inverter has taken a quick pace. To integrate solar PV to single phase grid for low power applications, it is required to track phase angle, amplitude and frequency of utility voltage vector and inverter output voltage. This can be done by using phase locked loop [2]. In the grid connected inverters the output parameters like voltage amplitude, frequency and phase angle are of greater importance to inject active and reactive power to the grid. In the case if inverters are fed from solar PV it can only supply active power to the grid. To supply reactive power, it

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needs a distributed static compensator (Dstatacom) [3] . In either of the situations to inject active and reactive power to grid decoupled controls of d-axis and q axis components of currents is employed and are controlled separately [3].

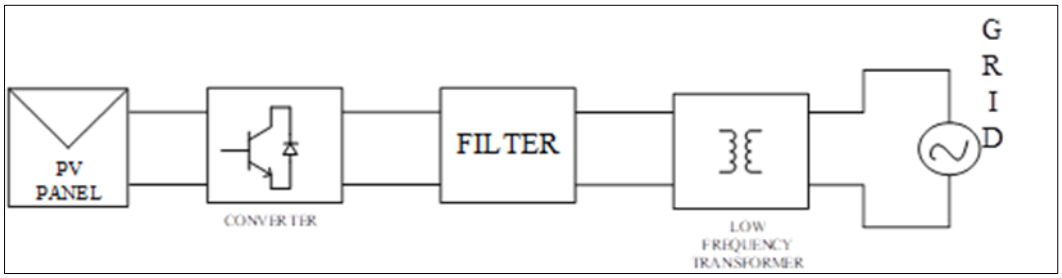

Figure 1 Grid connected inverter with low frequency Transformer

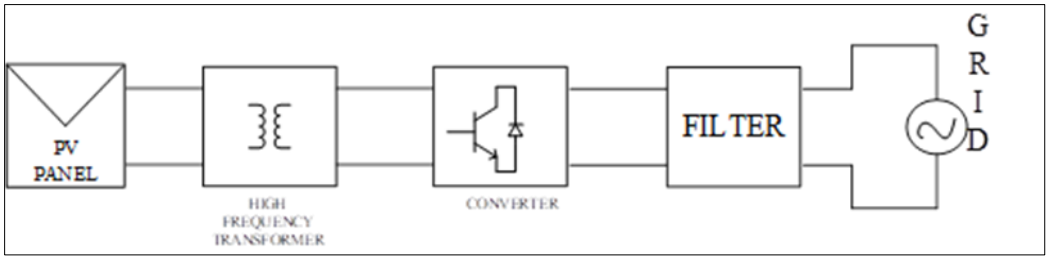

Figure 2 Grid connected inverter with high frequency Transformer

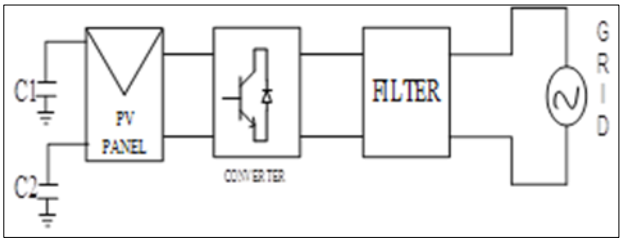

Figure 3 Transformerless Inverter

2. Phase locked Loop

Phase locked loop identifies and automatically sets phase angle of a voltage or current vector generated by an inverter with that of phase angle of grid voltage or current in grid connected system. The change in frequency of inverter which is required due to change in load can be adjusted with the help of PLL [4]. Besides various other techniques of synchronization of inverter to grid phase locked loop is simple in its implementation. The Figure.4 indicates block diagram of PLL based synchronization of transformerless inverter with grid.

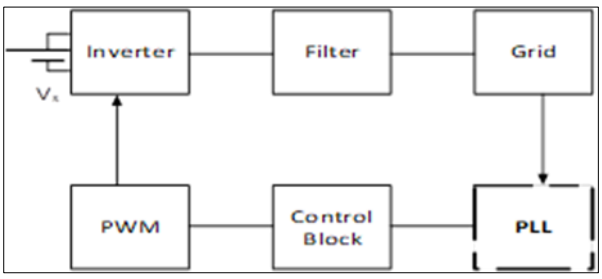

Figure 4 PLL based synchronization of transformerless inverter with grid

The basic PLL consists of Phase detector loop filter and controller along with a voltage control oscillator as shown in Figure. 5.Phase detector compares two input voltages generate an error signal that is proportional to the difference of phase angle between them. This error signal is fed to filter which will further drive voltage control Oscillator [5]. Thus, output is locked to phase at the input.

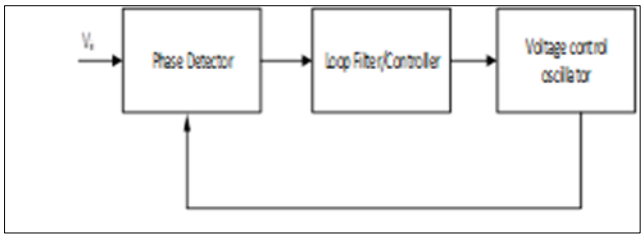

Figure 5 Block diagram of PLL

In the literature it has been stated that three phase PLL and single phase PLL are designed with different approach. Multiple techniques of synchronization of inverter to grid are surveyed out of which inverse park based PLL is the simplest.

It needs to generate a orthogonal component in single phase system unlike in three phase system, where inherently three phase system (a-b-c) can directly be converted into two phase orthogonal stationary reference frame system using Clarks transformation (α-β). Park transformation will convert stationary reference frame to synchronously rotating reference frame which are given by the following equations [6].

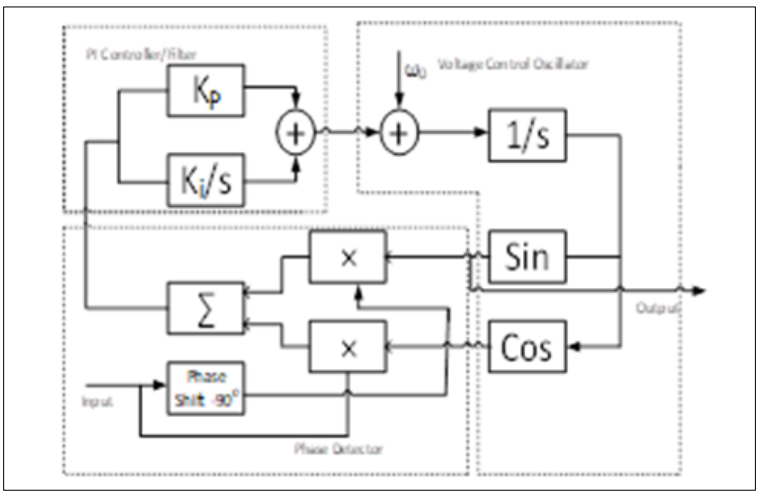

Figure 6 Mathematical modelling of PLL

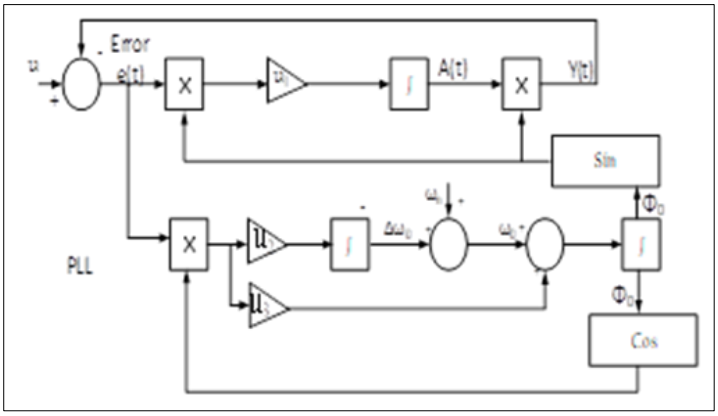

Figure 7 Block diagram of enhanced phase locked loop

Basic phase locked loop contains PI controller or filter , voltage controlled oscillator and phase detector as shown in Figure.6 The main focus of this paper is to present a comparison of basic phase locked loop structure with that of enhance phase locked loop in terms of their performances. Enhanced phase locked loop is found be best option for single phase grid connected systems. Further the steady state and dynamic performance of enhanced PLL is analyzed.[8].

3. Enhanced Phase locked Loop

The EPLL overcomes the disadvantage of basic PLL i.e double frequency error. This is done by estimating the amplitude of the input voltage or current signal with an extra loop. Besides EPLL removes double frequency error, it also gives filtered version of input quantity. In other words, EPLL not only acts as PLL but also as filter and controller which helps in direct measurement of phasor.

The lower portion of Figure.7. indicates basic PLL and upper loop indicates filtered input signal. Variables u1, u2 and u3 are positive gains to control the performance of EPLL [10]. Φ0 is estimated phase angle, ωn is reference frequency. In addition to constant estimate of fundamental component of input signal while the amplitude, frequency and phase are varying. It can also provide 900 phase shifted signal of fundamental component. Enhanced phase locked loop is best suited for single phase system whereas other techniques of synchronization like Recursive Discrete Fourier Transform, second order generalized integrator etc. [11]. Enhanced phase locked loop is characterized by the following equations in time domain.

$$A(t) = \int e(t).\sin\varphi_0(t).u_1.dt - - - - - (1)$$

$$\Delta\omega_0(t) = \int e(t).\cos\varphi_0(t).u_2.dt - - - - (2)$$

$$\varphi_0(t) = \int [e(t).\cos\varphi_0(t).u_3 + \Delta\omega_0(t) + \omega_n].dt \text{ -- } (3)$$

The error signal e(t) is the distortion of the input signal [12].

4. Simulink Modelling

This section shows the Matlab Simulink modeling of fundamental Phase locked loop and EPLL with changes in frequency [11]-[13]. The phase angle and frequency are shown . Figure.8. shows the Simulink model of basic PLL having a sinusoidal input with amplitude of 50 and frequency of 50Hz.

Figure.10. and Figure.11. indicates Simulink modeling of E PLL, which adds an extra loop for filtering the input signal so that fine control is possible [14]-[15].

The parameters like input amplitude, frequency, and typical values of gains u_1, u_2 and u_3 are shown in the following Table. 1

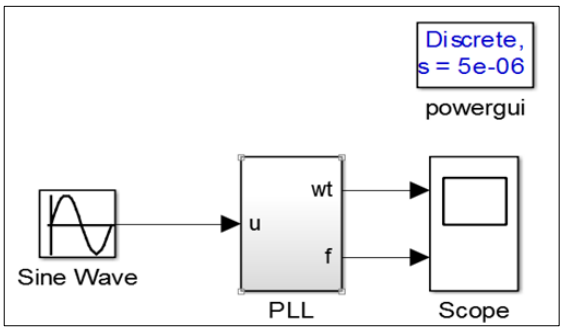

Figure 8 Simulink block diagram of PLL

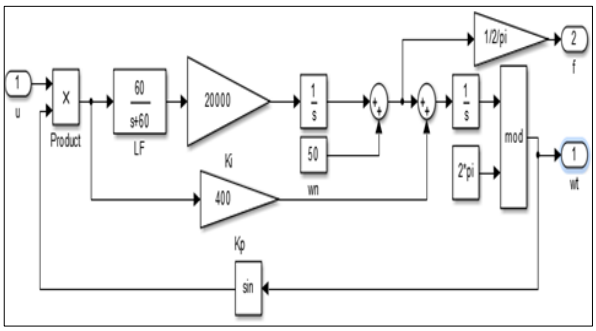

Figure 9 Mathematical PLL

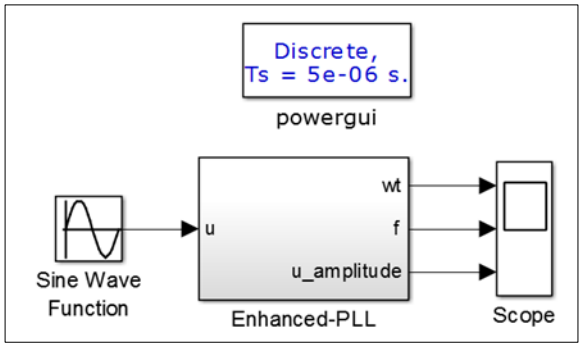

Figure 10 Enhanced Phase Locked Loop

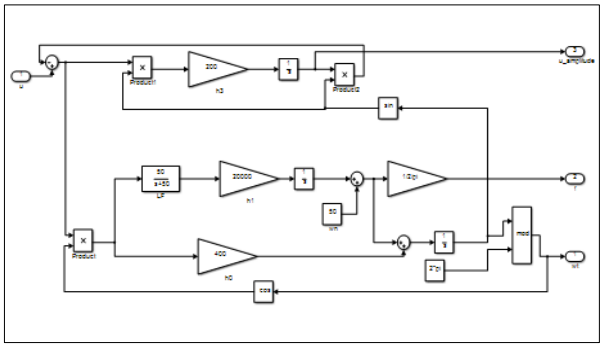

Figure 11 Mathematical equivalent of EPLL

Table 1 PLL Parameters

S. No	Fundamental PLL (Ts=5e-6)	
	Parameter	Value
1	Input voltage amplitude	230 Volts
2	Frequency	50Hz
3	Kp	400
4	Ki	2000
	EPLL(Ts=5e-6)	
1	Input voltage amplitude	230 Volts
2	Frequency	50Hz
3	u_1	200
4	u_2	20000
5	u_3	400

5. Results

The Simulink diagrams shown above indicates the operation of EPLL and fundamental PLL. The results of simulation of PLL and EPLL L are described and compared in the section 5.

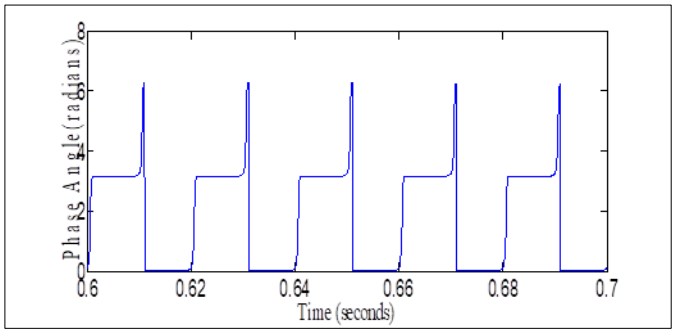

Figure 12 Phase measurement

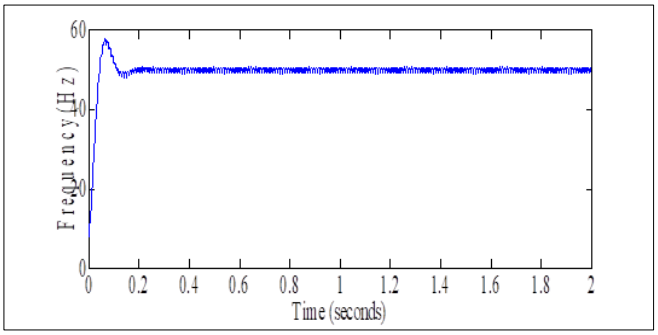

Figure 13 Frequency of basic PLL

The value of phase is shown n radians i.e. 6.28 as shown in Figure.12 The given signal frequency is found by PLL and is 50Hz as shown in Fig.13.

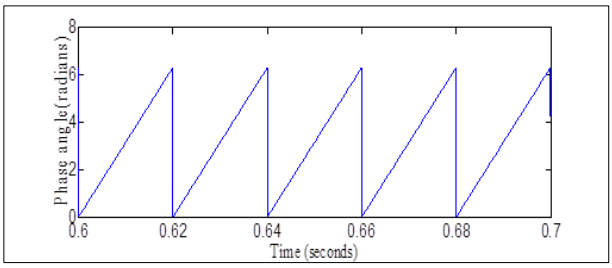

Figure 14 Enhanced Phase Locked Loop Phase

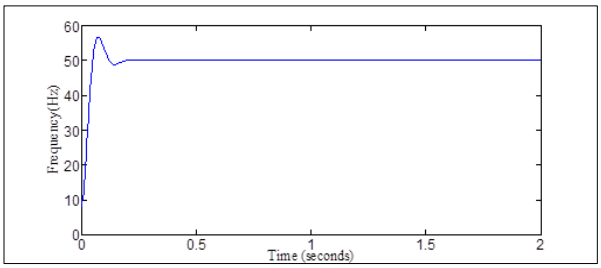

Figure 15 Enhanced Phase locked Loop Frequency

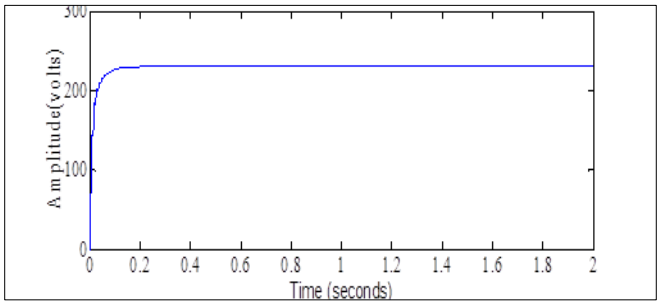

Figure 16 Enhanced Phase locked loop Voltage

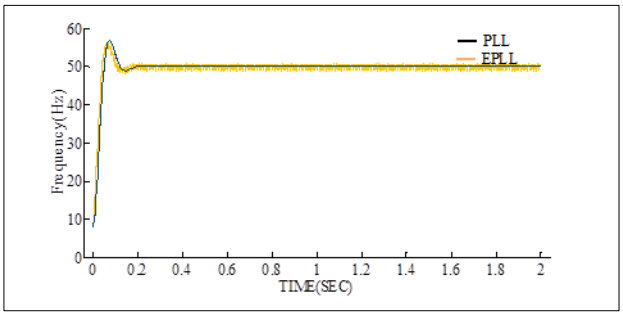

Figure 17 Frequency in PLL and EPLL

6. Conclusion

The phase angle, frequency and voltage amplitude of inverter output signal that is required to feed to grid has paramount importance in view of power control to the grid. By comparing Figure.12.and Figure.13. It is evident that the change of frequency in fundamental be more i.e. (3-5)Hz compared to the enhanced PLL has negligible (0.1 to 0.3 Hz) change is observed in its frequency measurements. Figure.11 and Figure 13. Shows the phase angle is not smooth in fundamental PLL compared to Enhanced PLL. In addition to accuracy , simplicity in implementation finds enhanced phase locked loop (EPLL) more prevalent in its usage when compared with other methods like synchronizing.

Compliance with ethical standards

Disclosure of conflict of interest

Three authors are involved in however no conflicts of interest.

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