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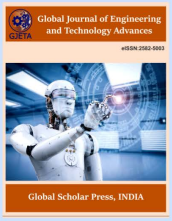

(RESEARCH ARTICLE)

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# Calibration of Cyclic-Pipelined ADCs Using CMOS for Area-Efficiency

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## Abstract

One of the principal obstacles in the development of pipeline analog-to-digital converters (ADCs) is the imprecision associated with residue amplification. Operational amplifiers (Op-Amps) that possess high gain and speed are recognized for their excessive power consumption, making them unsuitable for employment in proficient analog-to-digital converters (ADCs). The study presents a new method for foreground calibration that addresses amplification differences in cyclic-pipelined ADCs, reducing the need for internal amplifier DC gain. The calibration technique was applied to a cyclic-pipelined ADC with a sampling rate of 2 MS/s and 16-bit resolution. The design of this ADC was optimized for area efficiency, and its fabrication utilized 180 nm CMOS technology. The analog-to-digital converter (ADC) used a 5-bit resolution sub-ADC performing 4 cycles to reduce potential errors. Each cycle contained one bit of redundancy. A fixed-point iterative algorithm was used to find the exact gain for each amplifier. Simulation data shows a SINAD of 100. 6 dB, despite a 57 dB DC gain amplifier. The ADC's active area is 1. 8 mm2 at 30 consumption. 43 mW.

**Keywords:** ADC; 180 nm; Pipeline; Convertor; DC gain

## 1. Introduction

The application of condensing techniques in the context of analog-to-digital converters (ADC) is seeing an increase in demand, mainly due to their tendency towards extraordinary speed and accuracy in data acquisition. To ensure optimal performance, the amplifiers used in these converters must meet certain requirements in terms of characteristics such as speed, noise, and linearity. However, the task of designing amplifiers in the field of deep submicron technology poses serious challenges due to the limited transmission time and internal amplification of the device.

Digital calibration methods are widely used in the field of optimization. The purpose of this investigation is to clarify the concerns related to ADC and linearity and, furthermore, to reduce the impact of the result. The rest of the amplifiers follow strict specifications regarding their continuous power gain. A previous scientific publication [1] raised concerns about the presence of errors in the amplification process. The occurrence of this phenomenon can be attributed to the insufficient increase in the constant power of the remaining amplifier. The object in question is similar to the structure of the sound, which can interfere with the minimum. The telecommunications industry often uses a performance metric known as signal-to-noise distortion (SINAD) to evaluate signal quality ratings. Existing calibration methods have certain limitations in scope and efficiency. The tuning process using dithering methods is associated with suboptimal convergence speed. The literature emphasizes the need to apply approaches [2]–[4] to achieve high accuracy, as well as the requirement of slower speeds to achieve this result. The purpose of this study is to use the ADC to calculate the conversion errors that occur in the downstream stage of the ADC. The calibration technique based on the LMS (Least Mean Square) algorithm has already been documented in reference [5].

This study presents a new approach to forward signal calibration that effectively addresses issues related to residual amplification errors. The proposed methodology is cost-effective. The circular pipeline architecture explained in reference [6] is used to reduce the number of capacitors using hardware processing. A key feature of our methodology is the

continuous maintenance of all the remaining achievements in the sub-levels, which is facilitated by the use of integrated hardware implementation. This result leads to a superior solution for our calibration scheme. By implementing off-chip digital processing techniques, accurate measurement and correction of gain errors within amplifiers can be achieved.

## 2. An overview of the principle of the ADC circuit

### 2.1. Proposed ADC structure

The presented diagram illustrates the fundamental configuration of a cyclic pipelined analog-to-digital converter with the incorporation of single-bit redundancy, as portrayed in Figure 1. The primary procedure entails the utilization of capacitive circuits to take representative samples of the input signal and preserve them, followed by the transformation of the analog signal into a digital format via the deployment of an N-bit sub-ADC (SADC). The restricted length of digital signals can engender quantization errors and residual errors that give rise to substantial divergences between the original signals and their quantization levels. In order to enhance the precision of the conversion process, it may be advantageous to implement an amplification technique for error estimation and subsequently conduct the A/D conversion through the utilization of the "subtraction-amplification-A/D conversion" methodology.

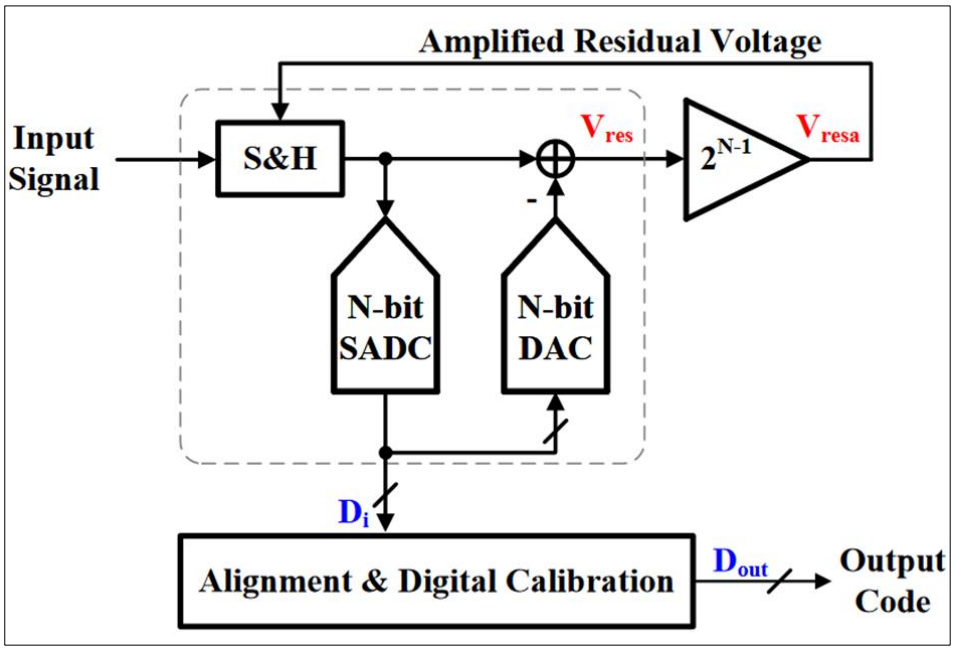


**Figure 1** Cyclic pipelined ADC with 1-bit redundancy has a basic structure

The illustration presented in Figure 2 depicts the arrangement of the proposed circuitry for the analog-to-digital converter (ADC). The system under consideration contains a semi-weighted capacitor register with 5-bit capacitance, a residual amplifier, a 6-bit signed analog-to-digital converter (ADC), and the necessary logic to ensure stable operation. The detection of residual faults in circuit capacitors is facilitated by utilizing a common node. Additionally, residual gain control can be achieved using an amplifier. The final analog-to-digital (A/D) output is computed by processing the digital code received from each substage using on-chip or off-chip methods. A major advantage of the analog-to-digital converters (ADCs) under consideration is hardware-based residual gain integration, which requires a single gain value across all substages, resulting in improved performance. The following sections illustrate the above-mentioned advantage.

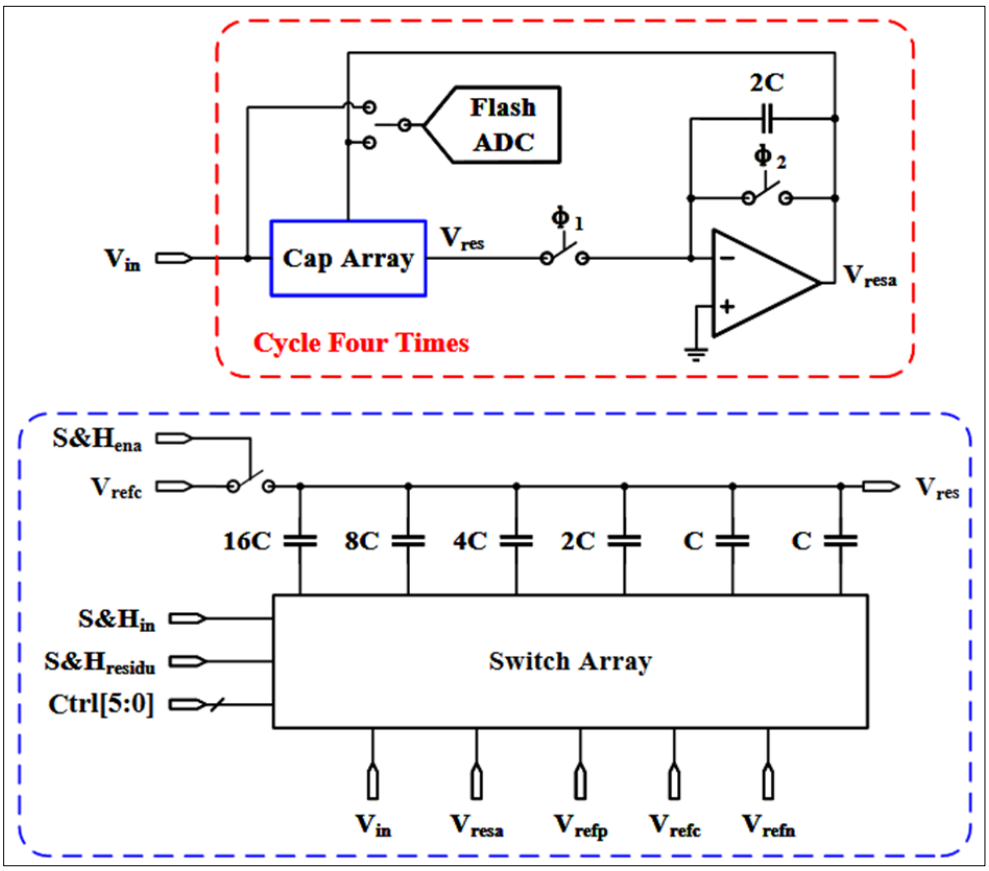


**Figure 2** Outline the ADC's design.

### 2.2. Requirements for residual amplifiers without calibration

A practical amplifier, unlike an ideal amplifier, has a finite gain, called Avol or open-loop gain. Insufficient reinforcement occurs as a result of the phenomenon mentioned above. Consequently, the resultant fluctuations in the output will unavoidably diminish the precision of the complete analog-to-digital conversion process.

In the context of amplification technology, an optimal amplifier is defined as an amplifier whose amplification result at each individual sublevel can be expressed as Vout,i = 2N -1 Vres,i, where N represents the sub-analog number of bits from the digital converter and the index i refers to the specific stage. Determining the derivative difference of the practical increment is done by the following method:

$$\Delta V_{out,i} = \frac{\left(2^{N-1}+1\right)\cdot 2^{N-1} V_{res,i}}{A_{vol}+2^{N-1}+1} \qquad (1)$$

To determine the final gain, a division operation must be performed in which the gain error is divided by a factor of 2i (N-1). The above observations show that the main reason for the decline in performance is due to profit errors that occur at the beginning. It follows that the total voltage swing, denoted as Vout,adc, can be calculated using the expression Vout, 1/2N-1.

Given that the initial input to the residual amplifier, denoted as Vres,1, is the difference between Vin and Vdac,1, it is possible to require that Vres,1 be divided by the same equation as Vres,1 U (0, VSLSB). Here, VSLSB represents the least significant bit (LSB) of the subframe. In this way, it is basic that the error within the yield adjusts to the dispersion of Vout,adc U(0, Q), with Q symbolizing the coefficient.

$$Q = \frac{\left(2^{N-1}+1\right) V_{ref}}{2\left(A_{ol}+2^{N-1}+1\right) 2^{N-1}} \qquad (2)$$

The overall performance of the system will be limited by both gain error and quantization noise, which are statistically unrelated variables. Therefore, the signal-to-noise ratio and distortion (SINAD) of the entire analog-to-digital converter (ADC) can be calculated.

$$SINAD = 20\log_{10}\left(\frac{V_{ref,rms}}{\sqrt{\Delta V_{out,adc,rms}^2 + V_{q,rms}^2}}\right) \quad (3)$$

The root mean square (RMS) of amplification errors, denoted as Vout,adc,rms, is commensurate with Q, whereas Vq, rms, is indicative of the RMS of quantization noise pervading the entire analog-to-digital converter (ADC) system. The depicted data in Figure 3 provides evidence that an inadequate DC gain of the residual amplitude leads to dominant amplification errors, which subsequently affect the quantization noise. As a result, a sine wave that maintains a linear relationship with respect to its DC gain is obtained. Moreover, it can be observed from Figure 3 that the mathematical analysis explicated in equation (3) is verified.

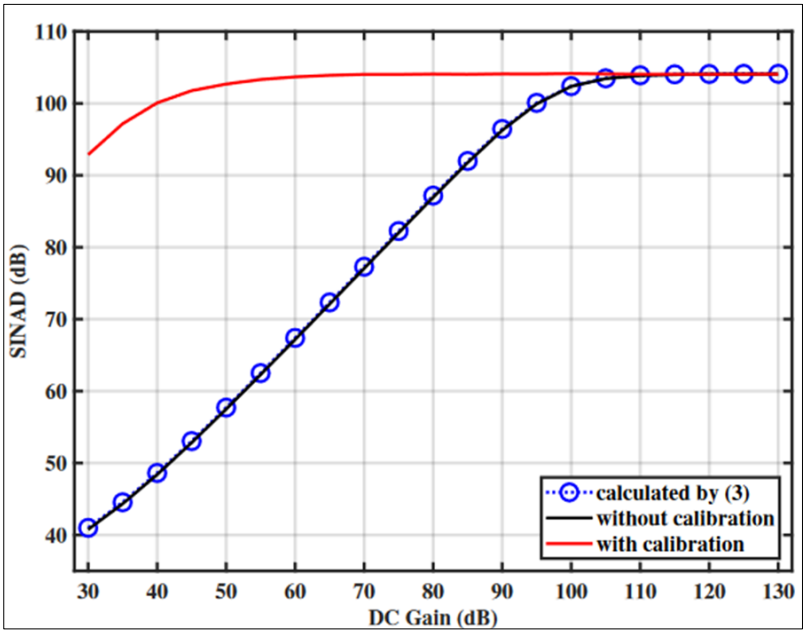


**Figure 3** Consideration of SINAD and DC gain for residual amplifiers is critical in a 4-cycle pipelined ADC, as low gain can limit performance.

## 3. Proposal for a calibration protocol

### 3.1. Basic calibration strategy

Although amplifiers have a high DC gain, it is not essential for reducing amplification errors. Assuming that all sub-stages have equal gains represented by 'G' due to using the same hardware, the A/D conversion result should be adjusted accordingly.

$$V_{out,adc,cali} = \frac{V_{ref}}{2^N}\sum_{i=1}^{M}\left(\frac{D_i}{G^{i-1}}\right) \quad (4)$$

The calibrated output voltage across the ADC is denoted by the symbols Vout, adc, and cali. Di, on the other hand, denotes the N-bit digital symbol produced by each substage of the A/D conversion. A significant reduction in gain errors can be achieved by using digital codes together with their respective gains when calculating the final result for each sub-stage. It is important to note that taking "G" during two consecutive analog-to-digital conversions can increase the resolution of the system by the order of "log2 G" bits. According to our design, using M = 4 cycles and N = 5 ADC subcircuits, we are able to calculate the effective number of bits (ENOB) that is theoretically possible.

$$ENOB = N + (M-1)\cdot\log_2(G) \quad (5)$$

According to the red line in Figure 3, it was observed that the amplifier with a constant gain of 40 dB can achieve a resolution of 16 bits, considering the gain of the G control. The focus of the investigation is to determine the precise control gain of the existing amplifier.

### 3.2. Estimate stage gain

Given the limitations of our analytical capacity in relation to circular structures, we have opted to broaden our examination of the data flow by utilizing the more conventional chain structure, as illustrated in Figure 4. The chain consists of two distinct constituents, namely the primary stage of the pipeline and the secondary component known as the analog-to-digital converter (ADC) or BADC. After the analog-to-digital conversion process, a residual voltage denoted by Vres1 is initially generated and then amplified through a gain factor denoted by G1. BADC performs an additional analog-to-digital conversion to determine the magnitude of the boosted residual voltage (G1Vres). To create the DBE feedback digital code, a process was developed to sum the digital codes obtained from each subphase, namely D2, D3, and D4.

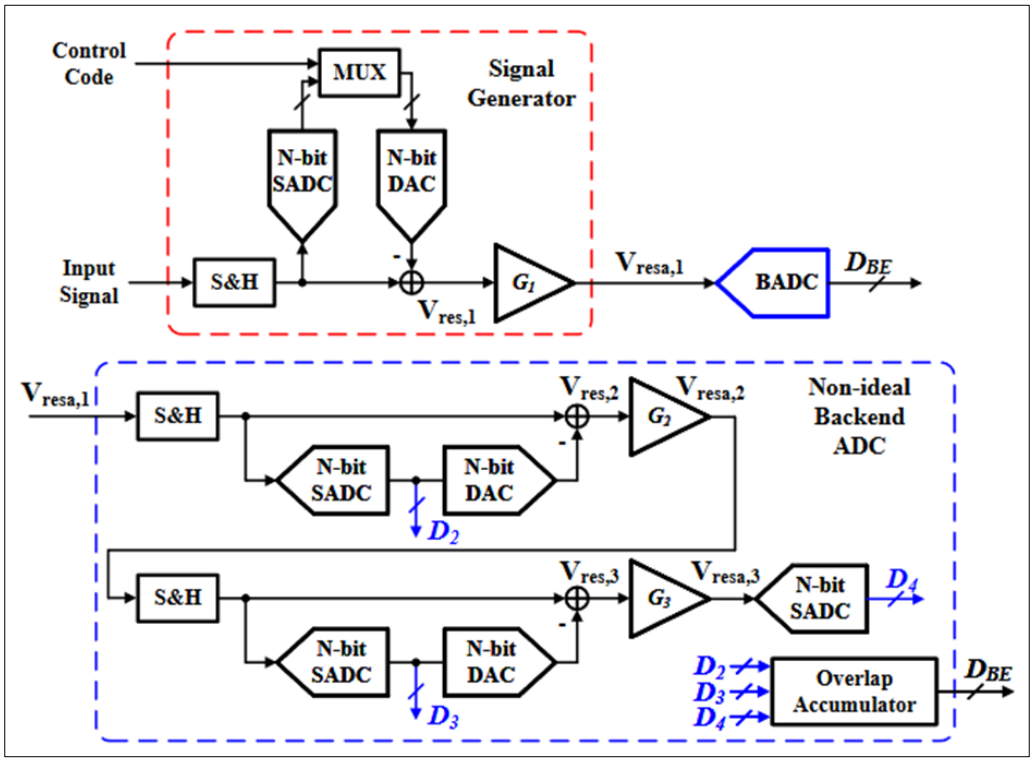


**Figure 4** The pipelined system consists of two components: the initial stage and BADC

Because our ability to analyze circular structures is limited, we chose to expand the data flow and assess it using the more conventional chain structure, as depicted in Figure 4. The chain is comprised of two separate components: the primary pipeline stage and the secondary analog-to-digital converter (ADC), also referred to as a BADC. The input signal Vin is kept at a constant amplitude, and two separate control codes are used throughout the MUX to obtain the remaining two signals. The above signals are amplified by G1 and then quantified using the Back-E technique.

$$D_{BE} = -\frac{2^{N_{BE}}}{V_{ref}} \cdot G_1 \left( V_{in} - \frac{Code}{2^N} V_{ref} \right) \qquad (6)$$

To prevent the increase in residual voltage G1 Vresi from exceeding the full scale range of BADC, it is important that the control codes Code and Vin are chosen carefully and widely. Following this principle, we set Win to 0, code (1) to 0, and code (2) to 1. Then we observe the inequality of the quantization results.

$$\frac{\Delta D_{BE}}{2^{N_{BE}}} = \frac{G_1 \times \Delta Code}{2^N} = \frac{G_1}{2^N} = \frac{G}{2^N} \qquad (7)$$

As we know, BADC quantization output consists of D2, D3, and D4, which can be written as:

$$\frac{\Delta D_{BE}}{2^{N_{BE}}} = \frac{1}{2^N}\left(D_2 + \frac{D_3}{G} + \frac{D_4}{G^2}\right) \quad (8)$$

$$G = D_2 + \frac{D_3}{G} + \frac{D_4}{G^2} \quad (9)$$

The numerical expression spoken to by condition (9) could be a cubic condition that as it were incorporates the variable G, which recognizes the evenhanded commitment of each sub-level. Moreover, it can be watched that this condition falls inside the genuine number set based on Banach's hypotheses.

### 3.3. Correct calibration accuracy

The solution to Equation (9) can be ascertained through the utilization of iterative techniques, namely fixed point iteration or Newton-Raphson iteration. This is graphically depicted in Figure 5. The computational resource requirements for achieving precision in function G are contingent upon the degree of accuracy sought. The following section will undertake an analysis of how alterations in the computed G value have an impact on the general resolution of the system. The process of calibration entails establishing the estimated interstage gain, denoted as G∗, which is equivalent to the actual gain GA, with the inclusion of the deviation parameter, ΔG. By utilizing numerical documentation in scholarly composing, the over condition can be communicated as G∗ = GA ± ΔG = GA (1 ± η). The variable η denotes the discrepancy between the observed and computed amplification. This formulation conforms to the style of academic writing. The information presented follows a formal methodology. The scientific notion of ΔG/GA delineates the alteration in Gibbs free energy (ΔG) with respect to the standard free energy (GA) for a particular reaction or system. Recognizing the importance of recognizing the inherent limitations of the η coefficient, it is essential to consider that it may encompass supplementary sources of inaccuracies, including calibrated systematic or random errors, imposed restrictions on the precision of calculations, and other assorted factors.

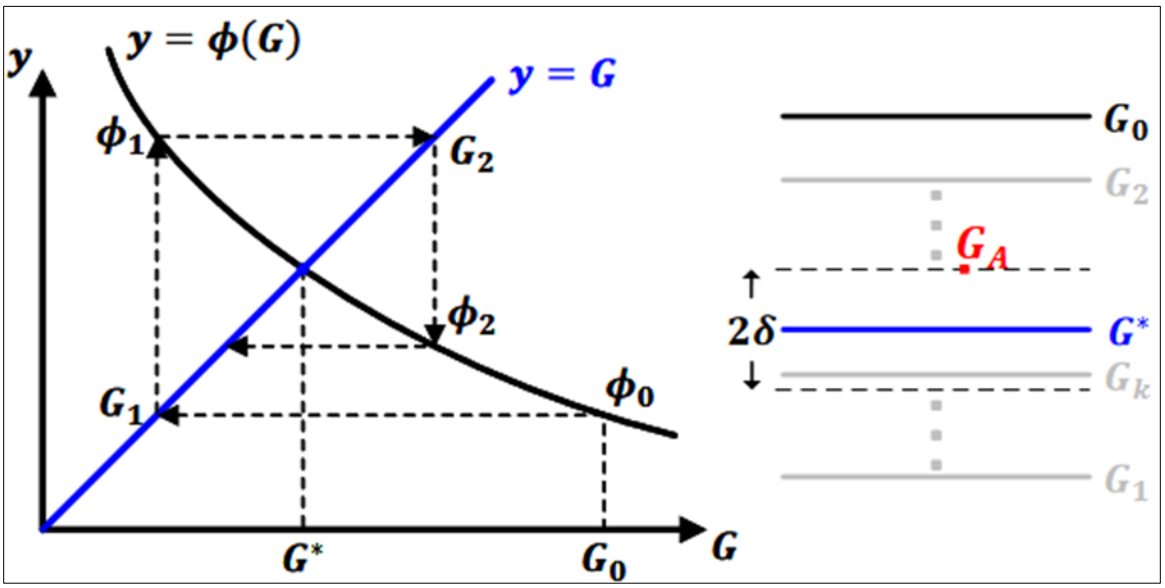


**Figure 5** G and G∗ in red and blue respectively are important indicators of a system's performance. Gk's gray color indicates the computed value after k iterations.

The root mean square (RMS) value can be used to express the collective gain error and quantization noise of the analog-to-digital converter (ADC).

$$\Delta V_{out,adc,rms} = \frac{1}{\sqrt{12}}\left[V_{ref} \cdot \frac{\eta}{2^N(1 \pm \eta)}\right] \quad (10)$$

$$V_{q,rms} = \frac{1}{\sqrt{12}}\left(\frac{V_{ref}}{2^{ENOB}}\right) \quad (11)$$

The abbreviation of SINAD can be obtained as follows:

$$|\Delta SINAD| = 10\log_{10}\left(\frac{\Delta V_{out,adc,rms}^2 + V_{\mathrm{q,rms}}^2}{V_{\mathrm{q,rms}}^2}\right) = 10\log_{10}\left(\alpha^2+1\right) \quad (12)$$

The determination of the coefficient was conducted by means of computing the relative root-mean-square (RMS) amplitude of the output discrepancy and quantization noise.

$$\alpha = \frac{\Delta V_{out,adc,rms}}{V_{q,rms}} = \left(\frac{\eta}{1\pm\eta}\right)\cdot G_A^{M-1} \approx \eta \cdot G_A^{M-1} \quad (13)$$

Using Equations (12) and (13) can help estimate the degradation of the accuracy of a common analog-to-digital converter (ADC). The above equations show that a larger relative error leads to a greater negative impact on the actual gain (GA) when it remains constant in absolute value.

The limited BADC solution creates a difference between the actual control gain GA and the value G determined by the calibration approach. Equation (7) can be used to estimate the maximum difference caused by the BADC solution.

$$\Delta G_{max} = \frac{2^N}{2^{N_{BE}}} = \frac{2^N}{2^{N+(M-2)\log_2 G_A}} = \frac{1}{G_A^{M-2}} \quad (14)$$

In addition, there is another inevitable factor that causes estimation errors. This factor is caused by the miscalculations that occur during the iterative algorithm, as shown in Figure 5. Considering the calculation errors introduced by the finite number of iterations, the highest deviation from the closed-loop gain will be Gmax. Additionally, the SINAD reduction can be calculated using the data in Figure 6.

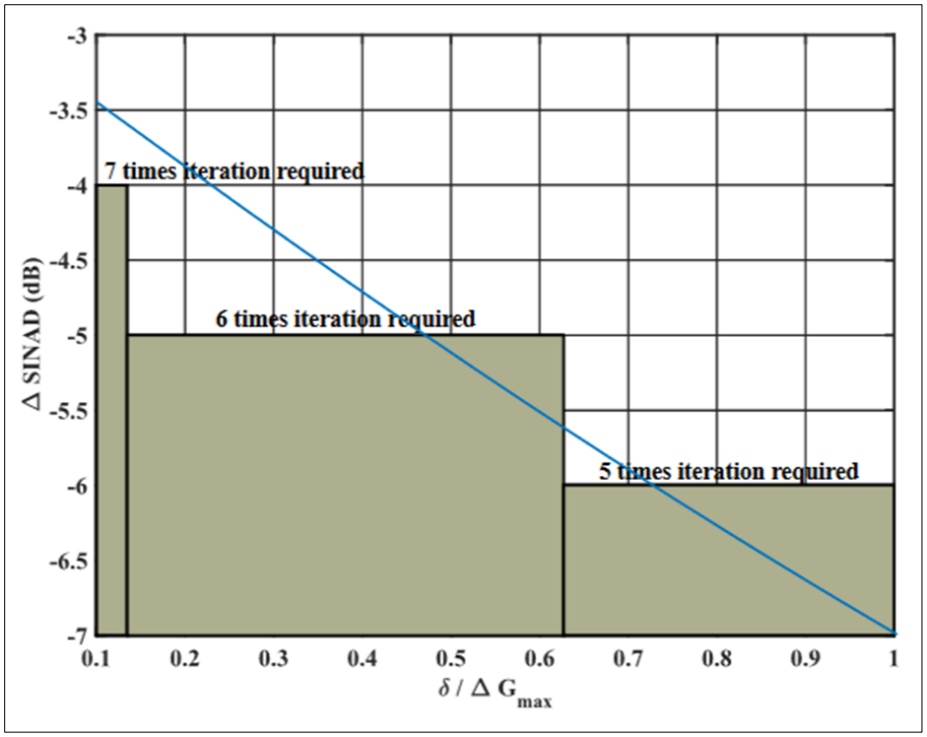


**Figure 6** Limited iteration and insufficient back-end resolution are key factors behind SINAD degradation.

Finally, after careful evaluation of calibration accuracy and power consumption, we decided to perform six iterations to correct the problem (9). As a result, a reduction in SINAD of about 3.6 dB was observed, which is considered within the acceptable range.

## 4. Results obtained from a simulation

The outcomes of the simulation are displayed in Figure 7. The experiment incorporated an input signal frequency of 167.968775 kHz and a sampling rate of 2 MHz. Following calibration, notable enhancements were observed in the spurious-free dynamic range (SFDR) and effective number of bits (ENOB) of the analog-to-digital converter (ADC). It is noteworthy that the preliminary measurements, measuring 73.08 dB and 10.8 bits, respectively, underwent a substantial escalation to 106.80 dB and 16.4 bits. The residual amplifier exhibited a power dissipation of 16.73 mW, whereas the flash analog-to-digital converter (ADC) and accompanying components exhibited power dissipation rates of 13.14 mW and 0.56 mW, respectively, for the entire analog-to-digital converter (ADC). In order to facilitate comparative analysis, pertinent studies are presented in Table 1.

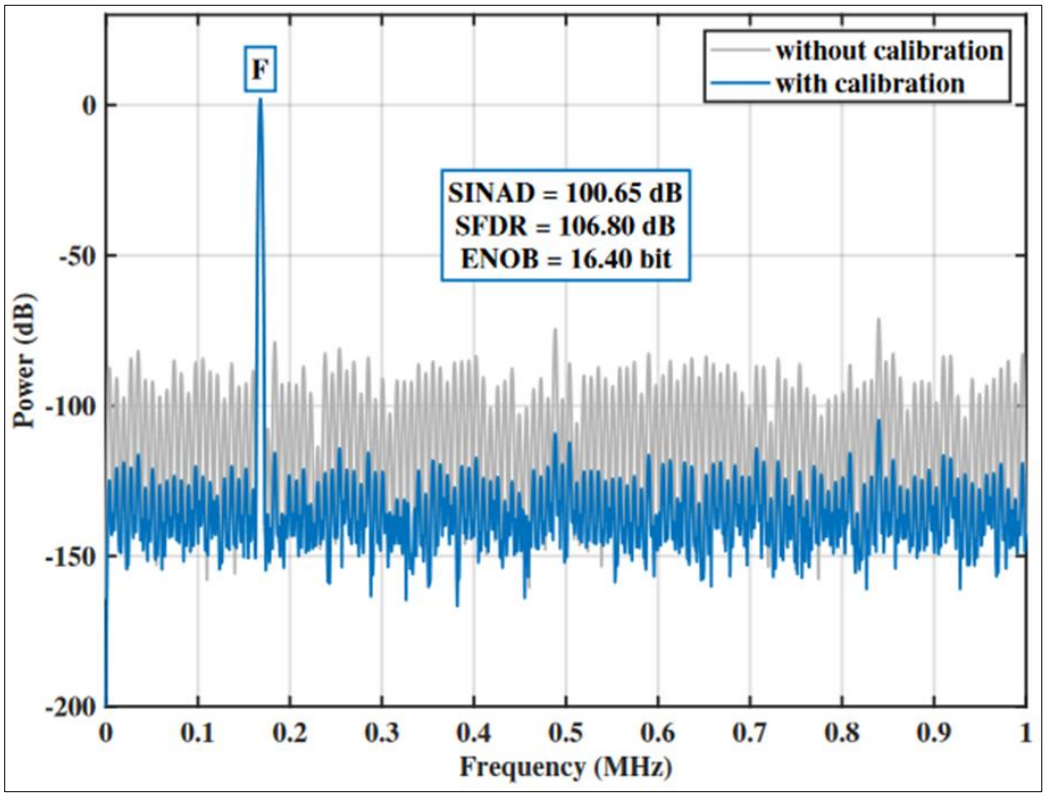


**Figure 7** The input signal's power spectrum was analyzed in two scenarios.

**Table 1** This paper compares performance measures

| | ENOB [bit] | SINAD [dB] | Power [mW] | Sampling Rate [MHz] | Supply [V] | Architecture | .Technology [nm] |
|---|---|---|---|---|---|---|---|
| our work | 16.4 | 100.65 | 30.43 | 2 | 1.8 | Cyclic | 180 |
| 1 | 13.62 | 83.92 | 0.059 | 0.1 | 3.3 / 1.2 | SAR | 130 |
| 8 | 13.76 | 84.6 | 0.00793 | 0.002 | 1.8 | Pipelined | 180 |
| 6 | 10.05 | 62.25 | 0.49 | 1 | 1.4 | Cyclic | 90 |
| 9 | 12.76 | 78.6 | 385 | 125 | 1.8 | SAR | 180 |

## 5. Conclusion

This paper introduces a methodology for achieving foreground gain calibration that effectively addresses the linear inaccuracies associated with inter-stage amplifiers within cyclic pipelined analog-to-digital converters (ADCs). Notably, this approach serves to mitigate the need for excessively high levels of direct current (DC) gain provision within said amplifiers. The Fix-Point Iteration algorithm is a pragmatic method that can facilitate the computation of the precise gain of individual amplifiers. Based on the simulation outcomes, it is apparent that a DC-gain amplifier of 57 dB has the ability to achieve a SINAD of 100.06 dB..

## Compliance with ethical standards

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*Disclosure of conflict of interest*

We hereby declared there is no conflict of interest.

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