Global Journal of Engineering and Technology Advances
eISSN: 2582-5003
Cross Ref DOI: 10.30574/gjeta
Journal homepage: https://gjeta.com/

(REVIEW ARTICLE)

Check for updates

Fast Detection and Precise Fault Localization Technique for DC Power Networks

Ali Taher Saber [1,*] Aland Faraidoon Ismael [2] and Ali Abed Zaidan [2]

[1] *Human Resources Section, College of Education for Humanities, University of Kirkuk, Kirkuk, Iraq.*
[2] *Independent Researcher in Electrical Engineering, Kirkuk, Iraq.*

Global Journal of Engineering and Technology Advances, 2026, 26(01), 196-204

Publication history: Received 14 December 2025; revised on 23 January 2026; accepted on 23 January 2026

Article DOI: https://doi.org/10.30574/gjeta.2026.26.1.0016

Abstract

DC distribution grids experience fault currents contributed by a wide range of distributed energy resources (DERs). Due to the inherently low impedance of tightly interconnected DC topologies, these currents escalate almost immediately once a fault occurs. Even though many power-electronic interfaces incorporate mechanisms to limit fault current, the regulated current profiles observed along various points of the network tend to be very similar, which severely restricts the effectiveness of protection methods that rely solely on current-magnitude differences. Consequently, DC networks require a protection approach capable of providing rapid, reliable fault detection and accurate fault localization.

This study presents a fault-location strategy that operates using only local electrical measurements and is specifically tailored for highly coupled DC architectures. The procedure determines , enabling swift fault clearing. The algorithm's performance and resilience are demonstrated through comprehensive numerical simulations as well as experimental validation on hardware.

Keywords: DC Power Networks; Fault Detection; Fault Localization; Inductance Estimation; Protection Systems

1. Introduction

Current developments in power-electronics technologies have increased the pace of transition to DC distribution in many areas of application. These include facilities in industrial processes, renewable-energy gathering circuits, electrical platforms on a ship board, data-centers with large infrastructure, and sophisticated systems of building-level distribution. These DC installations are still connected to standard AC grids so that power can be discharged in either direction between the local network and the bulk system.

In the event of a DC short-circuit, the resultant current is not provided by any single influential source, but rather a sum total of the utility interface, distributed generation units, embedded capacitance, energy-storage, and in most instances, controlled electronic loads. The combined effect of the resistance, inductance and capacitance along the path of occurrence of the fault determine the actual magnitude and temporal characteristics of the fault current.

One feature of DC systems is that it has an extremely low line impedance relative to analogous AC feeders. networks has very high performance requirements on the protection equipment including DC breakers, which are required to operate both fast and highly reliably. Resources (such as converters) are normally scattered across the system, and unless there is a well-coordinated deflection of protection, the potential short-circuit current through converter-dominated DC grids may run to several tens of kiloamperes - currents which can easily exceed the safe operating currents of semiconductor switching equipment.

* Corresponding author: Ali Taher Saber

Most converters use internal or actively controlled fault-current limiting (usually limited to about 1.5- times the rated current) but this so-called clipping has the effect of equalizing current distribution across the network. When these currents approach equal values then protection algorithms based on magnitude alone can no longer distinguish between upstream and downstream events and locating faults selectively becomes much harder.

Numerous fault-detection and fault-location strategies have been proposed for DC distribution systems, with impedance-estimation techniques receiving particular attention. One notable online inductance-estimation method infers the line inductance between a high-capacity local DC bus capacitor and a downstream fault by monitoring the transient response of both discharge. The method, however, presumes that the connected capacitor is sufficiently large to dominate the early-stage dynamics of the fault.

This assumption regarding the placement of a large measurement capacitor is often unrealistic in many parts of a DC network, limiting the method's applicability. A different technique relies on injecting a controlled capacitor-discharge into a section of the system that has been electrically isolated and powered down. By analyzing the resulting frequency components, the faulted distance can be inferred. Although technically informative, this strategy cannot be employed during normal operation because it requires the affected segment to be de-energized.

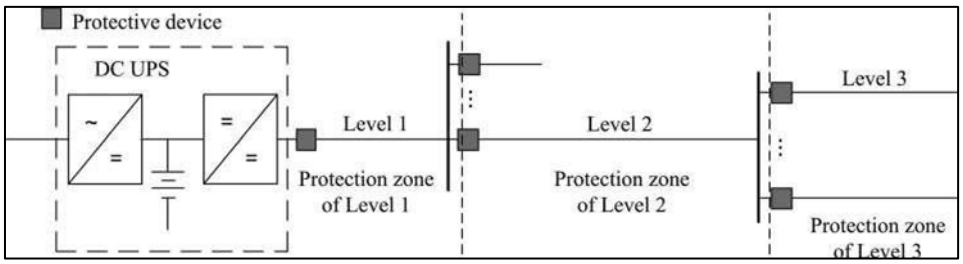

Figure 1 Conceptual single of a strongly coupled, illustrating the presence of low-impedance feeder paths, multiple converter-based generation and load interfaces

localization issue and analyses the effects of the properties of low impedance and strongly coupled DC structures on protection behavior. In Section III, the proposed local-measurement approach, which is grounded on voltage, current, and di/dt, is introduced and how inductive-distance estimation helps to provide coordinated protection without communication connections is explained. Section IV gives simulation studies that determine the responsiveness and sensitivity of the method and positional accuracy of the method.

Section V contains experimental validation of hardware testing and hardware-in-the-loop verification, which point to the possibility of real-life implementation. Section VI deals with practical implementation details and contains the description of limitations to the functioning of the method.

2. Problem Statemen

Figure 1 represents a standard DC distribution system, with a special AC/DC uninterruptible power supply (UPS) as one of its components.interface, feeder segments, various types of loads, and other protection devices used, including DC breakers. Though the DC/DC conversion stage in the UPS applies current-limiting control to limit the average current contribution by the fault, to the upstream, the discharge of the output capacitor is not controlled. This early surge can take over the early fault transient and may cause stress to attached constituents. Due to the very low impedances of DC networks, fault currents may reach their peaks in about 1 2 ms, and protective devices must act as quickly as possible to avoid damaging equipment and limiting the effects of faults to the entire system.

The total time to protection operation in a DC system as outlined in (1) includes a number of elements: the time needed to sense the fault, the time needed to locate the fault, any latency associated with communication lines (in the event of any use), and the interruption time that the protection device actually has.

$$t = t_{\{det\}} + t_{\{loc\}} + t_{\{comm\}} + t_{\{prot\}} (1)$$

Locally measured protection strategies become particularly appealing because of the avoidance of a latency introduced by communication. Rapid detection and rapid localization are important in such systems, particularly when it is coupled with swifter hardware. Every protective unit is permanently monitoring its own voltage and current indications and its

internal controller is running a high-rate algorithm that is used to decide whether the disturbance is within the intended protection area or not. In the event of the detection of an internal fault, the controller provides a trip command based not on external information, but on local measurements alone and capable of providing very fast fault-location and much more accurate positional estimates with reliable performance, without the communication links.

3. Innovative Method for Fault Detection and Location in DC Networks

Right after the fault initiation, there is a transient within the DC system that takes a few milliseconds. This transient response is used by the method to find the fault, by computing the equivalent inductance between the protection equipment and the faulted circuit.fault, with only locally available electrical signals. The parameter chosen as important is inductance since the real fault resistance is usually not known and does not greatly affect the accuracy of an inductance-based location estimate.

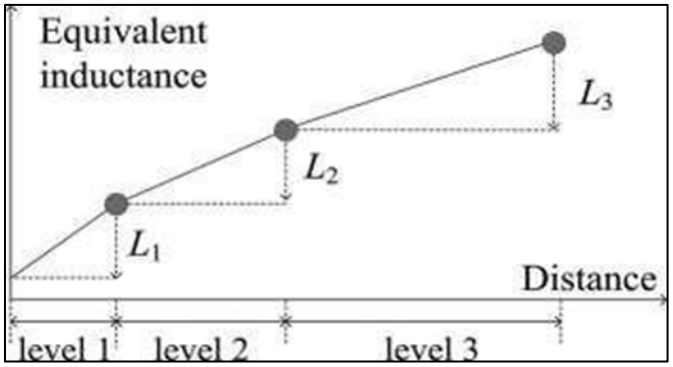

Figure 2 Estimated line inductances corresponding to system Levels 1 through 3

As illustrated in Fig. 1, the UPS fault-current limiter (FCL) activates shortly after a fault occurs. Because both communication latency and the internal response time of the FCL introduce delay, the upstream current remains uncontrolled for a brief interval before it settles to its regulated level. The proposed method utilizes this initial transient window: each protective unit records its locally measured The device measures local voltage, current, and di/dt signals and uses them to compute the equivalent inductance between its position and the fault. Figure 2 illustrates the inductive segments corresponding to protection Levels 1 through 3 (L1, L2, L3). If the calculated inductance is less than the predefined inductance of the device's protection zone, the fault is classified as internal.

Once an internal fault is confirmed, the local device sends a trip signal to isolate the affected section, allowing the rest of the network to continue normal operation. For estimation purposes, the simplified model in Figure 3 represents the line between the device and the fault using

representing the fault resistance. This model underlies the state-space formulation employed by the estimator. In practice, voltage, current, and di/dt measurements are captured at multiple time-stamped intervals during the transient, and the values of.

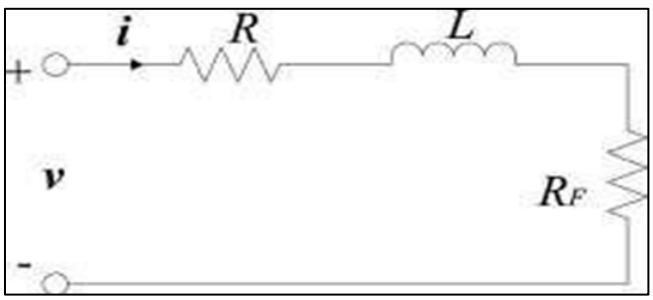

Figure 3 Illustrative comparison of SISFCL performance (a) passive configuration, (b) active configuration, and (c) impedance profile of a 35 kV SISFCL during current limitation

Figure 5 presents a simulation setup of a low-voltage DC network, including modeled converters, distribution feeders, loads, and protective elements. In this scenario, the inductance estimated at theLevel-3 breaker surpasses the upper

threshold for Level 3 but remains within the trip range of Level 4. As a result, Level-3 does not operate, while Level-4 successfully isolates the faulted section.

N denote the sampling index, and select a sampling interval between 20 μs and 100 μs based on the speed of the transient. Parameter values are then computed directly using a least-squares approach from the collected voltage, current, and di/dt samples.

$$.L \backslash frac\{di\}\{dt\} + \left(R + R_{\{F\}}\right), i$$

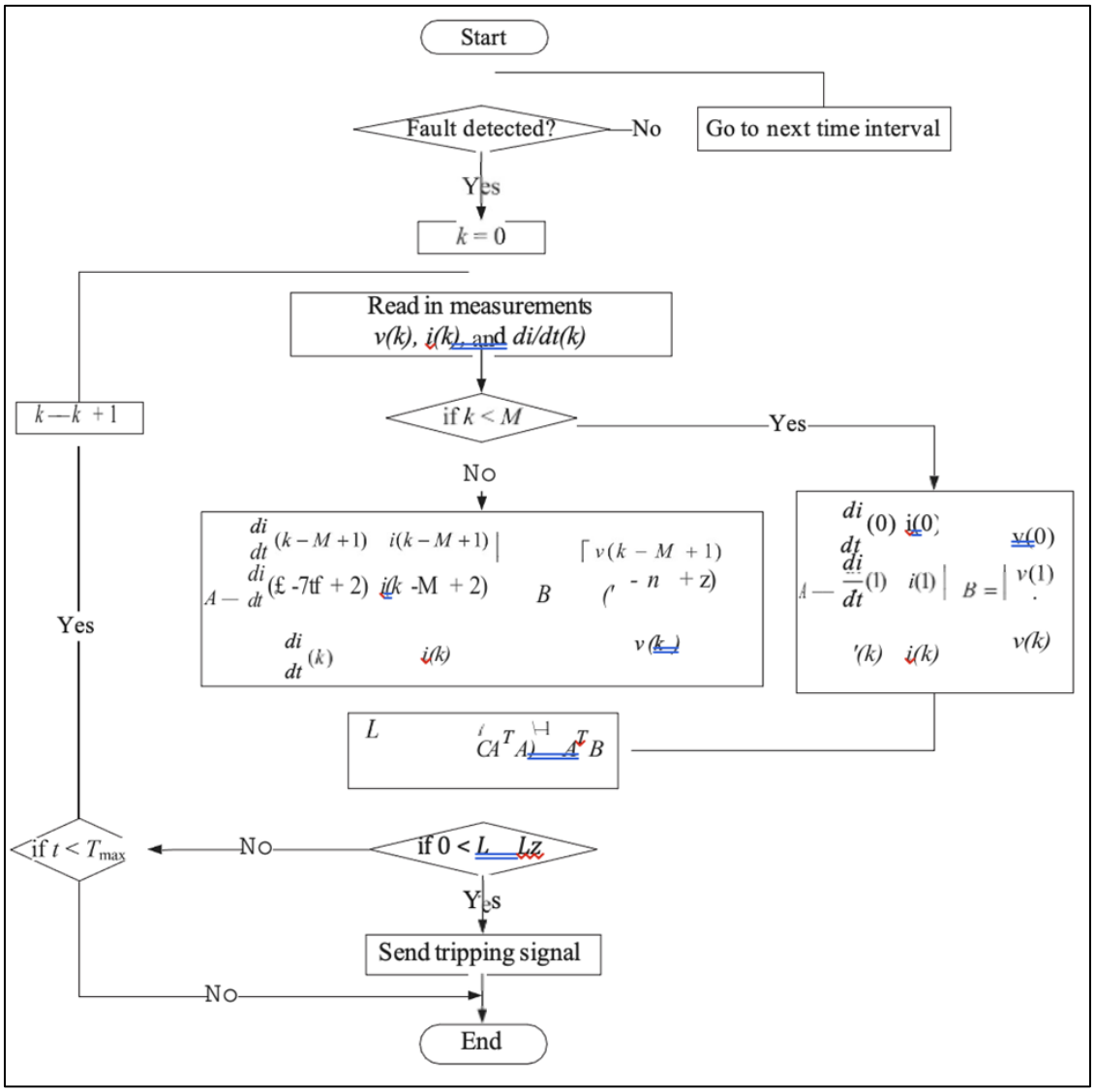

Figure 4 Flowchart of DC fault-location approach, showing transient signal measurement, computation of equivalent line inductance, classification of faults as internal or external, and activation of the protective trip command

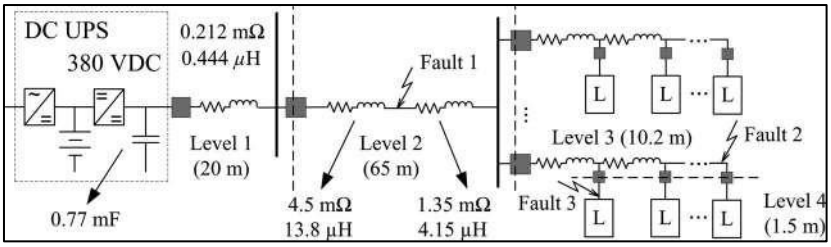

Figure 5 Simulation setup of a low-voltage DC (LVDC) distribution network, showing modeled converters, distribution feeders, loads, and protective elements. Parameter estimation is at

$$B = A \cdot \begin{bmatrix} L \\ R + R_F \end{bmatrix}, \text{ where } A = \begin{bmatrix} \frac{di}{dt}(0) & i(0) \\ \frac{di}{dt}(1) & i(1) \\ \vdots & \vdots \\ \frac{di}{dt}(N) & i(N) \end{bmatrix},$$

$$B = \begin{bmatrix} v(0) \\ v(1) \\ \vdots \\ v(N) \end{bmatrix}$$

Figure 6 Low-voltage DC (LVDC) distribution network

4. Numerical simulation

This section evaluates the proposed fault-location algorithm through numerical simulations. The low-voltage DC (LVDC) network is implemented in MATLAB/SimPowerSystems using a fixed time step of 0.005 ms, as illustrated in Figure 5. The UPS unit is rated at 100 kW with a 380 V DC output and includes a fault-current-limiting (FCL) feature that restricts the fault current to 1.5 times the nominal rating within approximately 0.6 ms after fault initiation. The network is arranged hierarchically: each Level-2 feeder supplies four Level-3 feeders, with each Level-3 feeder serving eight constant-resistance loads.

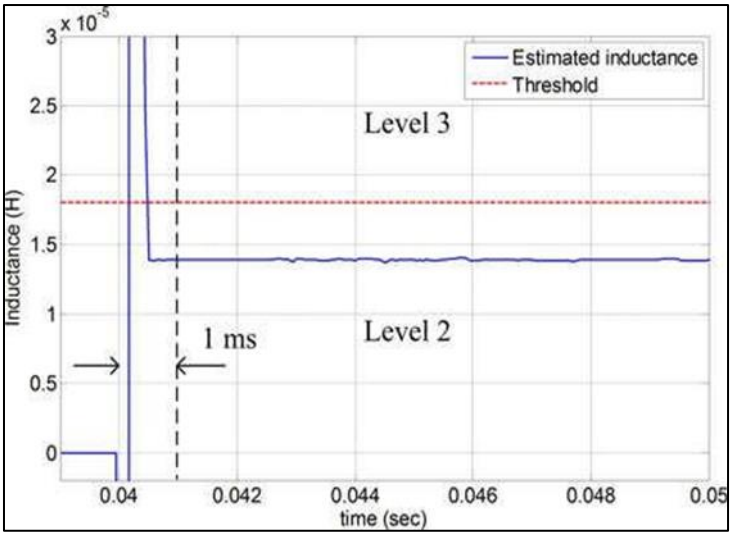

Figure 7 Calculated equivalent line inductance at the Level-2 breaker corresponding to Fault 1

Fault 1: A fault occurs at the far end of a Level-3 feeder. The equivalent inductance recorded at the corresponding Level-3 breaker (Figure 7) falls below its set threshold, prompting the Level-3 breaker to operate and isolate the affected section.

Fault 2: A fault is located downstream of a Level-4 breaker. To ensure proper discrimination between Level-3 and Level-4 events, a 2.5 μH boundary inductor is placed just upstream of each Level-4 breaker. This additional inductance adjusts the measured value at the Level-3 breaker, enabling accurate differentiation between faults on Level-3 and Level-4 feeders, as shown in.

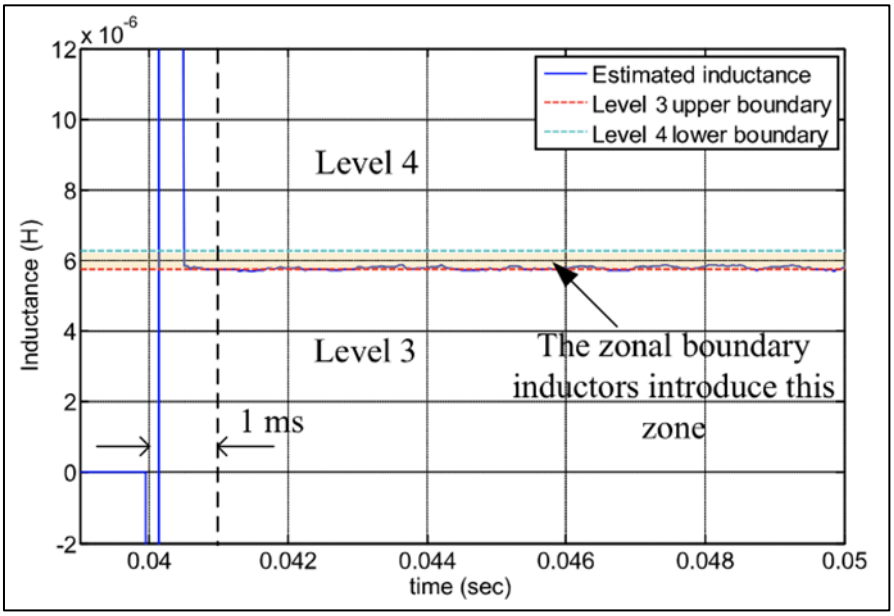

Figure 8 Calculated equivalent line inductance at the Level-3 breaker corresponding to Fault 2

detects the fault locations in the DC distribution system, and localizes them in less than 1 ms. Moreover, zonal boundary inductors would provide good discrimination on borderline cases, and proper selectivity between degrees of protection. These results, on the whole, prove that the inductance-based method allows achieving fast and reliable fault isolation without compromising the appropriate coordination of all the protection zones.

5. Experimental Validation Using Hardware-in-the-Loop (HIL) Testing

A scaled-down experimental setup, shown in Figure 9, is employed to validate the proposed approach. The test platform includes arepresented by either 6 μH or 12 μH. The converter stage is intentionally omitted since, during DC fault conditions, the capacitor's discharge dominates the current response. Consequently, only the filter capacitor and the relevant equivalent inductances needed to reproduce fault behavior are included. Before each test, the capacitor is precharged to 12 V DC to provide consistent initial conditions.

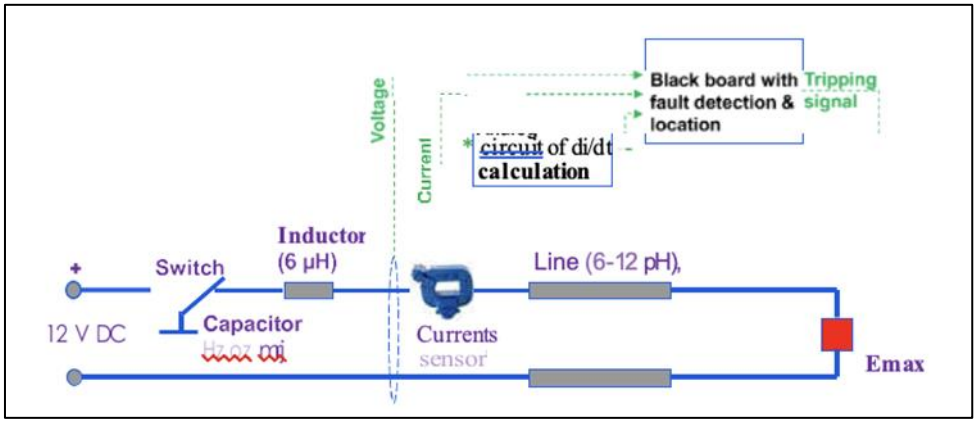

Figure 9 Schematic of the scaled experimental test circuit used for hardware validation

At the endpoint of the network, a protective device is deployed to separate faults. The method for locating anomalies[17] using magnetic properties operates on a freely available hardware platform[18] powered by a 1 GHz ARM Cortex-A8 chip.

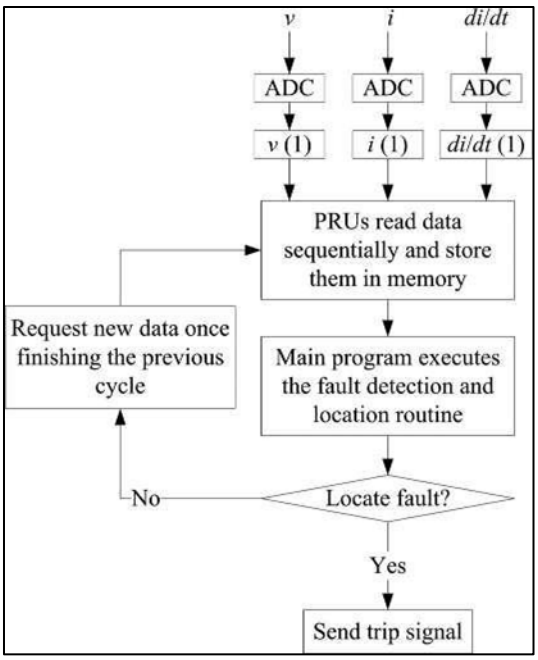

Figure 10 Deployment of the fault-detection and fault-location algorithm on the controller development board

positioned at the line origin measures [19] the current, while voltage is recorded at the same point. The di/dt signal is derived using an analog differentiator with appropriate The signals are processed through input and output filters. Each measurement is normalized to a 0–2 V range for direct digitization and later converted back to actual physical quantities in software. A fault is identified when current rises above a defined maximum or voltage drops below a specified minimum, which triggers the fault-location procedure. Oscilloscope recordings show that voltage falls immediately, the trip signal occurs about 0.7 ms after the fault, and current peaks near 0.4 ms. Over 15 experimental runs using two

different conductor lengths (see Table I), the inductance estimation error remained under 15 %, and the total detection and localization time did not exceed 0.75 ms.

6. Discussion

The total error in measurement is a combination of several factors: the di/dt stage provides an error of about 12-percent in total: noise amplification, bandwidth, and component tolerances causes it; the ADC and signal-conditioning stage contributes about 0.8-percent, and the current sensor contributes about 0.6-percent. The sensitivity analyses [14] indicate that a consistent fault localization is preserved when the current and the voltage measurement errors are current and voltage measurement errors respectively. Further enhancement of the accuracy is done by application of a well-constructed digital filter to the estimated inductance.

To enhance selectivity, small boundary inductors are placed at the interface of each protection zone, immediately upstream of the next device. These inductors help offset zone overlap measured noise. noise-induced error is near 12 %, a boundary inductor equal to approximately 12 % of the line inductance (with an additional safety margin) can be used. These inductors are small enough to have negligible impact on normal operation.

The method is intended for tightly coupled DC networks, including applications such as data centers, microgrids, commercial buildings, and shipboard power systems, where each line segment can be modeled using lumped resistance and inductance. When a feeder contains multiple types of cables, the overall equivalent circuit is formed by combining the R and L values of each cable to maintain accurate fault localization. For longer line sections, incorporating the equivalent capacitance is necessary to retain estimation precision. Research is ongoing to adapt this approach for DC networks with substantial cable capacitance.

7. Conclusion and future work

The reliance of inter-device communication, and its performance has been established by simulation as well as hardware-based testing. In all testing scenarios the technique attains sub-millisecond fault localization and detection as well as retaining the accuracy to do selective isolation. Future studies will be aimed at expanding the method to long-cable networks and mixed cable types and performing a computational di/dt calculation to minimise the measurement noise to achieve better inductance estimation and fault-location accuracy in general.

Compliance with ethical standards

Disclosure of conflict of interest

The Authors proclaim no conflict of interest.

References

[1] Short-Circuit Currents in D. C. Auxiliary Installations in Power Plants and Substations, Part1: Calculation of Short-Circuit Currents, IEC 61660-1. 1997.

[2] X. Feng, L. Qi, and Z. Wang, "Estimation of short circuit currents in mesh DC networks," in Proc. IEEE Power Energy Soc. Gen. Meeting, National Harbor, MD, USA, Jul. 2014, pp. 1-5.

[3] R. Cuzer and G. Venkataramanan, "The status of DC micro-grid protec-tion," in Proc. 2008 IEEE IAS Annu. Meeting, 2008, pp. 1-8.

[4] D. Ritchie, C. Booth, and J. Devlin, "Protection of future marine electrical systems," in Proc. 46th Int. Univ. Power Eng. Conf., Soest, Germany, 2011, pp. 1-6.

[5] J. P. Brozek, "DC overcurrent protection - where we stand," IEEE Trans. Ind. Appl., vol. 29, no. 5, pp. 1029-1032, Sep./Oct. 1993.

[6] S. D. A. Fletcher, P. J. Norman, S. J. Galloway, and G. M. Burt, "Determi- nation of protection system requirements for DC unmanned aerial vehicle electrical power networks for enhanced capability and survivability," IET Elect. Syst. Transp., vol. 1, no. 4, pp. 137-147, Dec. 2011.

[7] L. Qi and J. Liang, "Design issues and practical application challenges of DC shipboard distribution system protection," in Proc. 2015 IEEE Elect. Ship Technol. Symp., Alexandria, VA, USA, 2015, pp. 403-408.

[8] P. Cairoli and R. A. Dougal, "New horizons in DC shipboard power systems," IEEE Electrif., vol. 1, no. 2, pp. 38-45, Dec. 2013.

[9] F. Yang, X. Zhang, J. Zhuang, and C. Dai, "Shipping distribution networks short circuit selective protection method based on fast recovery power breaker" in Proc. 2011 Asia-Pacific Power Energy Eng. Conf., 2011, pp. 1-5.

[10] S. D. A. Fletcher, P. J. Norman, S. J. Galloway, and G. M. Burt, "Optimiz-ing the roles of unit and no-unit protection methods within DC microgrids,' IEEE Trans. Smart Grid, vol. 3, no. 4, pp. 2079-2087, Dec. 2012.

[11] J. E. Hill, S. D. Fletcher, P. J. Norman, and S. J. Galloway, "Protection system for an electrical power network," U.S. Patent Application US 20120200966 A1. Jan. 26, 2012.

[12] J. D. Park, J. Candelaria, L. Ma, and K. Dunn, "DC ring-bus microgrid fault protection and identification of fault location," IEEE Trans. Power Del., vol. 28, no. 4. pp. 2574-2584, Oct. 2013.

[13] J. D. Park, "Fault detection, isolation, location and reconnection systems and methods," U.S. Patent Application US 20130286521 A1, 2013.

[14] X. Feng, L. Qi, and J. Pan, "Fault inductance based protection for DC distribution systems," in Proc. 13th Int. Conf. Develop. Power Syst. Pro-tection, Edinburgh, Scotland, Mar. 2016, pp. 1-6.

[15] X. Feng, L. Qi, and J. Pan, "A novel fault location method and algorithm for DC distribution protection," in Proc. 2016 IEEE Ind. Appl. Soc. Annu. Meeting, Portland, OR, USA, Oct. 2016, pp. 1-5.

[16] L. Ljung, System Identification: Theory for the User, 2nd ed. Englewood Cliffs. NJ, USA: Prentice-Hall, 1998.

[17] SACE Emax 2 New low voltage air circuit-breakers, ABB Inc., Mar. 2013. [Online]. Available: http://new.abb.com/docs/librariesprovider- 22/technical-documentation/emax2.pdf

[18] R. P. J. Day, "Beaglebone black system reference manual revision C.1," Texas Instruments, Dallas, TX, USA, May 2014. [Online]. Available: http://elinux.org/Beagleboard:BeagleBoneBlack

[19] "LEM Current Transducer HO-S series," LEM, Jul. 2014. [Online]. Avail-able: http://www.lem.com/docs/products/ho-s_series.pdf