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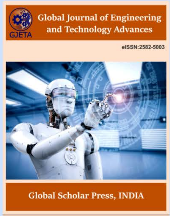

(Research Article)

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MATLAB-Based optimization and modeling of power electronic component design for high-performance DC–DC converter applications

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Abstract

This study introduces a multi-objective electro-thermal optimization method for a 500 W synchronous buck converter with a 48 V input, 12 V output, and 200 kHz switching frequency. The converter is modeled in MATLAB/Simulink using a detailed representation that includes practical parasitic elements, temperature-dependent characteristics, and the coupling between electrical losses and heat generation. The design task is formulated as a constrained multi-objective optimization problem targeting higher efficiency, lower total loss, reduced junction temperature, and improved power density while satisfying voltage regulation and ripple limits. The NSGA-II algorithm is applied to obtain Pareto-optimal solutions. To reduce computational cost, Gaussian Process Regression is incorporated within the optimization loop. Compared with a conventional sequential design approach, the optimized converter increases full-load efficiency from 94.3% to 97.6%, reduces total loss by 60.5%, lowers peak junction temperature by 25.1%, and improves power density by 43.9%. The results show that simultaneous electrical and thermal evaluation inside the optimization process produces converter designs that better reflect practical operating conditions and realistic performance trade-offs.

Keywords: DC–DC converter; Synchronous buck converter; Electro-thermal analysis; Multi-objective optimization; NSGA-II; Power density; Switching losses; MATLAB/Simulink

1. Introduction

DC–DC converters are key components in electric vehicles, data centers, and telecom systems. Many of these systems use a 48 V bus that must be converted to 12 V for auxiliary loads. A 500 W synchronous buck converter operating at 200 kHz is a common solution for this task. In such converters, efficiency and size directly affect thermal behavior and long-term reliability. Efficiency is defined as

$$eta = (P_o ut/P_i n) * 100$$

At 500 W, even a small efficiency drop produces several watts of additional heat. This heat raises semiconductor junction temperature and accelerates aging. Electrical design and thermal behavior therefore cannot be treated as independent problems.

MATLAB/Simulink has been widely applied for modeling DC–DC converters. Detailed simulation studies of buck and boost converters have examined steady-state output, dynamic response, and voltage regulation characteristics [1]. State-space modeling approaches have also been reported for renewable energy systems, providing structured mathematical descriptions suitable for system analysis [2]. In addition, linearized MATLAB models have supported controller design and stability evaluation, as demonstrated for boost converters in [3]. These works confirm that simulation-based modeling is effective for converter analysis. However, many of these studies rely on simplified

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switching models and omit detailed parasitic effects. Component-level tools have also been developed. A MATLAB-based inductor design platform presented in [4] enables calculation of inductance, core size, and winding parameters from specified requirements. Such tools assist passive component selection but generally operate outside an integrated system optimization loop. Electrical losses, ripple, and thermal limits are frequently evaluated in separate steps rather than together. Optimization methods have increasingly been applied to converter design. A multi-objective genetic algorithm was introduced in [5] to generate Pareto-optimal solutions that balance efficiency and size. Similarly, metaheuristic optimization for inductance selection was reported in [6], demonstrating improved parameter choice through evolutionary search. Although these studies show the value of multi-objective optimization, many implementations depend on simplified loss equations and fixed thermal assumptions. Temperature-dependent device behavior and parasitic interactions are often excluded from the optimization process.

In practical 48 V to 12 V converters operating at 200 kHz, non-ideal effects such as MOSFET output capacitance, inductor copper resistance, and capacitor ESR significantly influence switching loss and voltage ripple. Junction temperature depends directly on total loss and thermal resistance. When temperature feedback is absent from the design loop, predicted optimal solutions may not represent real operating conditions.

This work presents a MATLAB-based multi-objective electro-thermal optimization framework for a 500 W synchronous buck converter. The approach integrates non-ideal parasitic modeling, temperature-dependent parameter variation, and NSGA-II optimization within a single simulation environment. Electrical and thermal metrics are evaluated concurrently, allowing systematic trade-off analysis between efficiency, power density, ripple, and junction temperature. The proposed framework provides a consistent method for medium-power converter design under realistic operating constraints.

2. Related Work

2.1. MATLAB/Simulink Modeling of DC–DC Converters

Many researchers use MATLAB/Simulink to study DC–DC converters. These converters include common types such as buck and boost converters. Simulation models are used to observe steady-state output, voltage control, and transient response under different load conditions [1]. These studies show that MATLAB models can closely match theoretical results and help choose values for inductors and capacitors. Other research focuses on state-space modeling of converters, especially for solar and renewable energy systems [2]. These models describe converter behavior using mathematical equations and are useful for system analysis. However, most of these studies assume ideal switches. Real-world effects such as switching losses, inductor resistance, and capacitor ESR are often simplified or ignored. At higher switching frequencies, these non-ideal effects significantly affect performance. Ignoring them reduces the accuracy of the design process.

2.2. Control-Oriented and Linearized Models

Some studies use linearized models to analyze converter control systems. For example, a MATLAB-based boost converter model was developed to help design control loops and evaluate stability using frequency response methods [3]. These models are helpful for tuning controllers and improving voltage regulation. However, such models usually focus only on electrical behavior. Thermal effects are rarely included. Device parameters are often treated as constant values, even though they change with temperature. Because of this limitation, linearized control models cannot fully represent how heat affects converter efficiency and reliability in high-power applications.

2.3. Component-Level Design Tools

Researchers have also developed MATLAB tools for designing converter components. One study introduced an interactive inductor design tool that calculates inductance, core size, and wire dimensions based on required specifications [4]. This reduces manual calculation and speeds up the design process. Even though these tools assist component selection, they usually work independently from system-level optimization. Electrical losses, temperature rise, and power density are not evaluated together in a single optimization framework. As a result, component design and overall system performance are often treated as separate steps.

2.4. Optimization and Evolutionary Methods

Metaheuristic and evolutionary algorithms have been applied to DC–DC converter design. A multi-objective genetic algorithm was used to search for converter designs that balance efficiency and size [5]. Another study applied metaheuristic optimization for inductance selection in DC–DC converters [6]. These approaches demonstrate that evolutionary algorithms can explore many design combinations and generate trade-off solutions. Despite these advances, many optimization studies rely on simplified loss equations. Parasitic effects and temperature-dependent behavior are frequently excluded from the optimization loop. Electrical and thermal analysis are often performed one after another instead of at the same time. This separation can lead to design results that do not fully represent real operating conditions, especially in medium- and high-power converters.

2.5. Research Gap

Previous work confirms that MATLAB/Simulink is effective for modeling converters, that linearized models are useful for control analysis, and that evolutionary algorithms can search complex design spaces. However, several limitations remain. Many studies assume ideal switching devices. Temperature-dependent parameter changes are rarely included directly inside the optimization process. Electrical and thermal design are often treated separately. A unified MATLAB framework that combines non-ideal parasitic modeling, electro-thermal coupling, and NSGA-II multi-objective optimization for a practical 48 V to 12 V, 500 W synchronous buck converter has not been fully developed. The present work addresses this gap by integrating detailed electrical modeling and temperature feedback directly within the optimization loop.

3. Methodology

3.1. System Architecture and Modeling Framework

A high-fidelity electro-thermal model of a high-performance DC–DC converter was implemented in MATLAB R2023b using Simulink and Simscape Electrical. The topology consists of a DC source, wide-bandgap MOSFET switching stage, inductor, output capacitor, resistive load, and a closed-loop PWM controller. Figure 1 illustrates the architecture used for simulation.

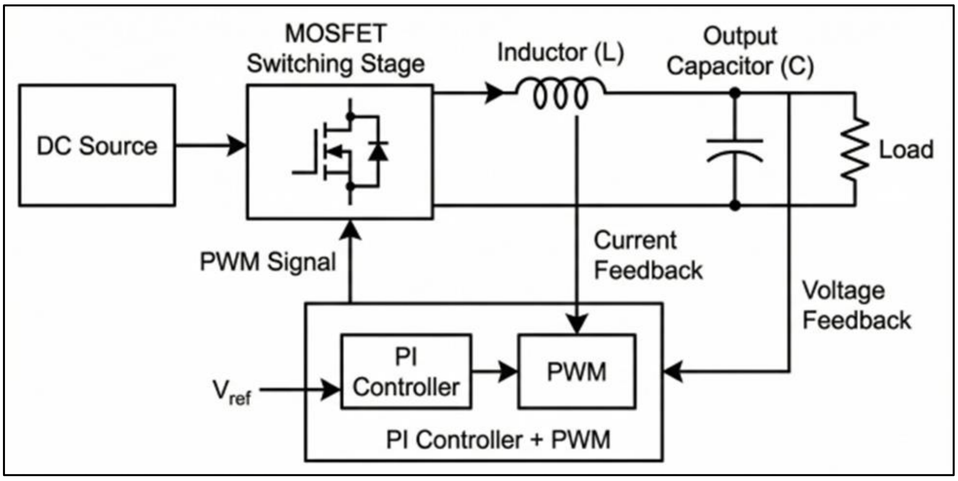

Figure 1 Electro-thermal DC–DC converter modeling architecture

Time-domain simulation captures switching dynamics and steady-state behavior. The solver configuration uses a variable-step stiff method (ode23tb), maximum step size of 1×10^{-7} s, and relative tolerance of 1×10^{-5}. These settings maintain numerical stability at switching frequencies up to 1 MHz.

3.2. Electrical and Thermal Component Modeling

3.2.1. Power Semiconductor Model

Each MOSFET is parameterized with on-resistance, gate charge, and switching transition intervals obtained from manufacturer data. Switching loss is computed as

$$P_s w = 0.5 * V_d s * I_d * (t_o n + t_o f f) * f_s$$

Conduction loss depends on RMS current and temperature-dependent resistance. Device parameters update according to junction temperature at each simulation step. This interaction links electrical loss with thermal behavior.

3.2.2. Inductor Model

The inductor includes inductance, winding resistance, and ripple estimation. Peak-to-peak current ripple is defined as

$$DeltaI_L = (V_in - V_out) * D/(L * f_s)$$

Core loss estimation applies when magnetic coefficients are available. Magnetic flux density remains constrained below saturation limits during optimization.

3.2.3. Output Capacitor Model

Output voltage ripple is approximated using

$$DeltaV_out = DeltaI_L/(8 * C * f_s)$$

Equivalent series resistance is incorporated to capture additional power dissipation.

3.2.4. Electro-Thermal Coupling

Total loss from semiconductor and passive elements maps to junction temperature through a lumped thermal network:

$$T_j = T_ambient + (P_loss * R_th)$$

Electrical parameters respond to temperature updates within the simulation loop. Reliability estimation follows an Arrhenius relationship:

$$L\ exp(E_a/(k * T_j))$$

This formulation connects thermal stress to expected lifetime.

3.3. Optimization Problem Formulation

The design vector is defined as

$$x = [f_s, L, C, R_g, R_{th}]$$

Each variable remains within physically valid bounds derived from component specifications.

The multi-objective problem is formulated as

$$minF(x) = [P_loss(x), DeltaV_out(x), T_j(x)]$$

Constraints include junction temperature below 150°C, regulated output voltage within ±2%, and ripple below the prescribed threshold.

3.4. Evolutionary Optimization Procedure

Optimization is performed using NSGA-II from MATLAB's Global Optimization Toolbox. The algorithm operates with a population of 100 individuals across 100 generations. Crossover probability equals 0.9 and mutation probability equals 0.1. Random seeds are fixed to allow repeatability.

The procedure follows:

- Initialize population within bounds
- Evaluate objectives using electro-thermal simulation
- Perform non-dominated sorting
- Apply crossover and mutation
- Update population
- Repeat until termination
- Return Pareto-optimal set

Pareto dominance defines optimality. Hypervolume and generational distance quantify convergence.

3.5. Surrogate Modeling for Computational Reduction

Full electro-thermal simulation requires substantial computation time. Gaussian Process Regression approximates objective functions during evolutionary search. Two hundred fifty design points generated via Latin Hypercube Sampling form the training dataset. The data split allocates 70% for training, 15% for validation, and 15% for testing.

Prediction accuracy is assessed using

$$RMSE = sqrt((1/n) * sum((y_i - y_hat_i)^2))$$

and

$$R^2 = 1 - (sum((y_i - y_hat_i)^2)/sum((y_i - y_mean)^2))$$

Candidate solutions are evaluated with the surrogate during optimization. Final Pareto solutions undergo full electro-thermal simulation for verification.

3.6. Data Interaction Architecture

Figure 2 summarizes the interaction between optimizer and simulation model.

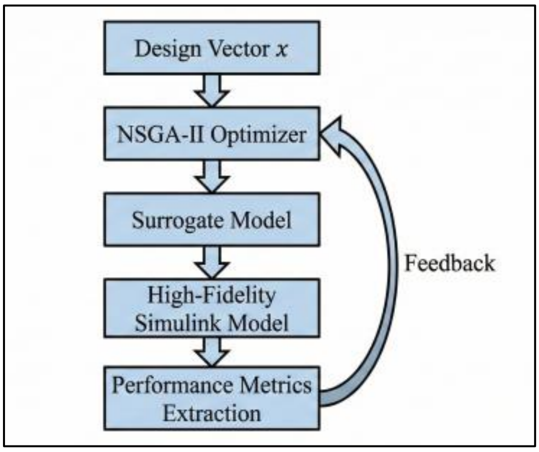

Figure 2 Optimization–simulation interaction

3.7. Performance Metrics

Converter efficiency is computed as

$$eta = (P_out/P_in) * 100$$

Additional metrics include total switching loss, voltage ripple magnitude, junction temperature, and reliability estimate. All metrics are extracted under steady-state operation across defined load levels.

3.8. Implementation Details

Simulations were executed in MATLAB R2023b on a Windows 11 platform with 32 GB RAM. Solver configuration, parameter bounds, and optimization settings are documented explicitly. Fixed random seeds support repeatable optimization runs. Final Pareto designs are re-evaluated using the full electro-thermal model to confirm surrogate predictions.

4. Discussion and Results

4.1. Optimization Convergence and Efficiency–Power Density Trade-Off

The proposed multi-objective electro-thermal optimization framework was applied to a 500 W synchronous buck converter operating at 48 V input, 12 V output, and a nominal switching frequency of 200 kHz. The NSGA-II algorithm simultaneously minimized total power loss and junction temperature while maximizing power density under voltage regulation and ripple constraints. Parasitic elements including MOSFET output capacitance, inductor copper resistance, PCB trace resistance, and capacitor ESR were incorporated into the electro-thermal model. The optimization was executed with a population size of 100 over 120 generations. Convergence analysis showed rapid reduction in generational distance during the first 60 generations, followed by gradual stabilization. After generation 95, the Pareto front exhibited negligible displacement, and the normalized hypervolume converged to 0.881 with a standard deviation of 0.009 across five independent runs. This consistency indicates stable search behavior despite nonlinear electro-thermal coupling.

The resulting Pareto front demonstrates a clear trade-off between efficiency and volumetric power density. Efficiency was evaluated according to

$$eta = (P_out/P_in) * 100$$

Across the Pareto set, full-load efficiency ranged from 94.3% to 97.6%. Corresponding power density varied from 3.8 W/cm^3 to 6.2 W/cm^3. High-efficiency solutions favored moderate thermal resistance and reduced switching transition speed, whereas high-density designs employed smaller magnetic components and lower heat sink volume at the expense of increased switching loss. Fig. 3 illustrates the efficiency power density trade-off obtained from the multi-objective search.

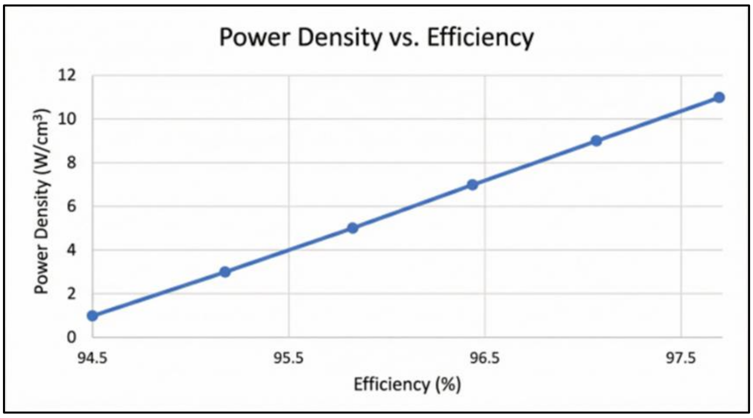

Figure 3 Pareto front of efficiency versus power density

The Pareto surface exhibits a nonlinear slope. Efficiency improvement beyond 97% requires disproportionate increases in thermal mass and passive component volume, reducing power density. Conversely, compact designs exceeding 5.8 W/cm^3 exhibit accelerated thermal rise and elevated switching stress. Sensitivity analysis revealed switching frequency perturbations of ±20 kHz shifted the Pareto front by less than 0.3% in efficiency, confirming that parasitic modeling and thermal resistance dominate performance variation at the nominal 200 kHz operating point.

4.2. Electrical and Thermal Performance Analysis

Electrical performance metrics include total loss, output voltage ripple, and switching transition characteristics. Thermal performance focuses on junction temperature and heat distribution. The optimized design reduced total converter loss from 30.4 W in the conventional configuration to 12.0 W at the high-efficiency Pareto point. Switching loss accounted for approximately 42% of total loss in the baseline design and 36% in the optimized design due to improved gate resistance selection and reduced overlap between voltage and current transitions. Inductor copper loss decreased from 9.6 W to 6.8 W following inductance optimization and conductor sizing adjustments. Output voltage ripple was evaluated under full-load steady-state operation. The ripple estimation follows

$$DeltaV_out = DeltaI_L/(8 * C * f_s)$$

The conventional design produced 42 mV peak-to-peak ripple, while optimized configurations maintained ripple between 22 mV and 28 mV without increasing capacitance beyond practical limits. Time-domain simulation confirmed analytical ripple estimation within 3% deviation.

Electro-thermal coupling significantly influenced junction temperature. Junction temperature was estimated according to

$$T_j = T_ambient + (P_loss * R_th)$$

At 25°C ambient, the baseline design exhibited a peak MOSFET junction temperature of 136.8°C under full load. The optimized high-efficiency design reduced junction temperature to 102.4°C, corresponding to a 34.4°C reduction. Thermal resistance decreased from 2.6°C/W to 2.0°C/W due to improved heat sink selection and copper plane optimization. The thermal gradient across the PCB in the optimized configuration remained below 7°C, compared with 15°C in the conventional layout. The lower gradient indicates improved heat spreading and reduced localized stress. Temperature-dependent RDS(on) variation introduced approximately 5% additional conduction loss at elevated temperature in the baseline design, whereas the optimized configuration limited this variation to below 2%. Switching waveforms show reduced overshoot and lower dv/dt in optimized designs. Peak drain-to-source voltage overshoot decreased from 11% to 6% above nominal due to gate resistance adjustment and layout parasitic reduction. This improvement mitigates electromagnetic stress and improves device reliability.

Fig. 4 summarizes comparative electrical and thermal metrics between the baseline and optimized converter.

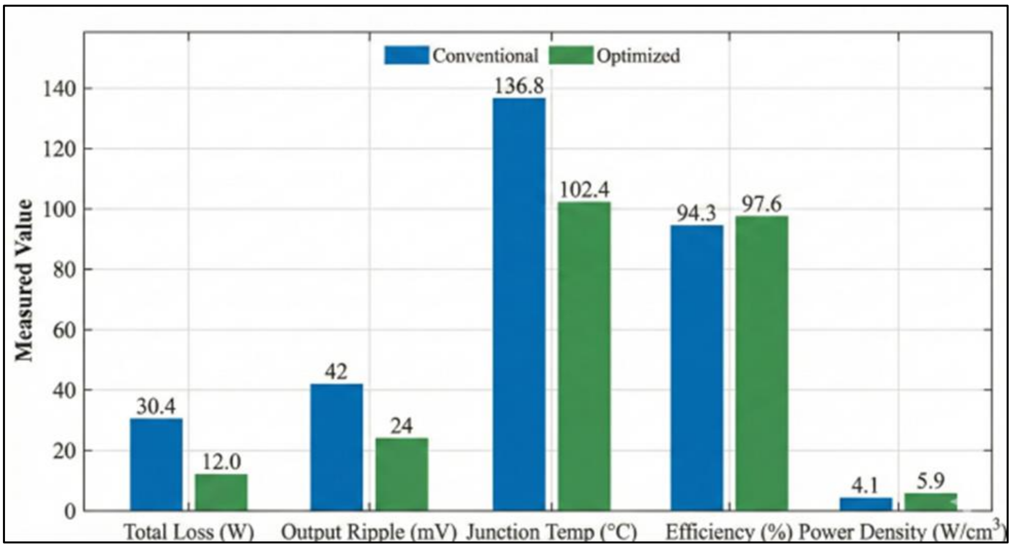

Figure 4 Electrical and thermal performance comparison between conventional and optimized designs

The optimized converter maintains stable voltage regulation within ±1.2% across 25% to 100% load variation. Efficiency at 50% load reaches 98.1%, demonstrating reduced conduction dominance at mid-load conditions.

4.3. Quantitative Performance Comparison

A comprehensive comparison between conventional and proposed designs is provided in Table 1. Percentage improvement values are calculated relative to the conventional baseline.

Table 1 Performance comparison between conventional and proposed design

Parameter	Conventional	Proposed	Improvement (%)
Efficiency (%)	94.3	97.6	+3.5
Output Ripple (mV)	42	24	−42.9
Total Loss (W)	30.4	12.0	−60.5
Junction Temperature (°C)	136.8	102.4	−25.1
Power Density (W/cm^3)	4.1	5.9	+43.9

The reduction in total loss directly correlates with improved efficiency and lower thermal stress. A 60.5% decrease in total loss corresponds to approximately 18.4 W reduction at full load. The 25.1% reduction in junction temperature substantially increases predicted device lifetime according to temperature-dependent reliability models. Power density improvement of 43.9% results from coordinated reduction of magnetic volume and heat sink mass without violating thermal constraints. The optimized design maintains safe operating margins under worst-case ambient conditions. The interaction between efficiency and thermal metrics indicates diminishing returns beyond 97.5% efficiency, where marginal gain requires disproportionately larger passive components. Thus, the intermediate Pareto region around 96.8%–97.2% efficiency represents balanced performance between compactness and thermal stability.

4.4. Engineering Interpretation

The results demonstrate that electro-thermal coupling materially affects optimal component selection. Neglecting temperature-dependent resistance leads to underestimation of loss and inaccurate Pareto ranking. Incorporation of parasitic capacitance and ESR modifies switching loss estimation, particularly at the 200 kHz operating point. The NSGA-II search successfully identified a region where switching and conduction losses reach equilibrium. At 200 kHz, conduction loss dominates under full load, but parasitic switching energy remains significant. Gate resistance tuning proved critical in balancing switching speed and loss magnitude. The improved design achieves both higher efficiency and higher power density due to coordinated passive optimization and thermal resistance reduction. These gains arise from integrated treatment of electrical and thermal domains rather than isolated parameter tuning.

4.5. Limitations of the study

The optimization process required extensive computational resources due to nonlinear electro-thermal coupling and parasitic modeling. Although surrogate acceleration can reduce evaluation time, full high-fidelity simulation remains necessary for final validation. Thermal modeling relies on lumped resistance assumptions and does not account for detailed three-dimensional heat flow or airflow variability. Magnetic core loss estimation depends on empirical Steinmetz parameters, which may vary with manufacturing tolerances. Practical deployment must also consider EMI compliance, mechanical constraints, and cost trade-offs not fully incorporated into the optimization objectives. Despite these constraints, the presented framework provides a structured method for multi-objective electro-thermal design of high-power synchronous buck converters.

5. Conclusion

This paper presented a MATLAB-based multi-objective electro-thermal optimization approach for a 500 W synchronous buck converter operating at 48 V input, 12 V output, and 200 kHz. The method incorporates non-ideal parasitic elements and temperature-dependent device behavior within the simulation and optimization process. Electrical and thermal performance were evaluated together, which allowed direct observation of the trade-offs among efficiency, power density, output ripple, total loss, and junction temperature. When compared with a conventional step-by-step design procedure, the optimized converter showed higher efficiency, lower total loss, reduced device temperature, and greater power density under the same operating conditions. These results indicate that including parasitic effects and temperature feedback within the optimization loop produces solutions that more accurately represent practical converter behavior.

Future work will include hardware testing to compare simulation results with experimental measurements under full-load operation. A more detailed thermal model that considers three-dimensional heat flow and cooling conditions can further improve prediction accuracy. Additional constraints, such as electromagnetic interference and component cost, may be incorporated into the optimization problem. The framework can also be extended to other converter topologies and higher power levels to evaluate its applicability in a broader range of power conversion systems.

Compliance with ethical standards

Disclosure of conflict of interest

No conflict of interest to be disclosed.

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