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DESIGN AND SIMULATION OF A 10-BIT SUCCESSIVE APPROXIMATION REGISTER ADC WITH A BOOTSTRAPPED SAMPLING SWITCH IN 180 NM CMOS

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ABSTRACT

This paper describes a 10-bit successive approximation register (SAR) ADC designed in Cadence Virtuoso and simulated with Spectre on the 180 nm gpdk180 process. The converter has a bootstrapped sampling switch, a binary-weighted charge-redistribution capacitor DAC (10 fF to 5.12 pF), a StrongARM latch comparator, a 12-state SAR controller and a 10-bit output register, all driven by one 1 MHz, 5 V clock. The transistor-level cells were checked one by one, and the whole converter was checked with Verilog-A behavioural models. A conversion takes 12 clock cycles, giving 12 µs, 83.3 kS/s and a 4.883 mV LSB. With a 10 kHz, 2.5 V ± 0.1 V sine input, bits D9 to D0 come out in order, the output register loads only on the register clock, and the output lags the input by one conversion. The recorded output matches an ideal quantiser in all 40 conversions. INL lies between −0.33 and +0.50 LSB, DNL between −0.42 and +0.39 LSB, there are no missing codes, the SNR is 33.7 dB and the ENOB is 9.95 bits. The kT/C noise of the 10.23 pF array is 20.1 µV rms (0.4% of an LSB).

Keywords: SAR ADC, Charge Redistribution, Capacitive DAC, Bootstrapped Switch, Strongarm Latch, Verilog-A, Mixed-Signal Design, Gpdk180

1 INTRODUCTION

Almost every signal that a system senses, such as temperature, pressure, a bio-potential or sound, is analog, while processing, storage and communication are digital. Analog-to-digital converters (ADCs) sit at this boundary and link sensors, audio and radio front ends to digital processors [8]. Every ADC trades speed against resolution, and published

designs spread along a well-known envelope [5], so the first design choice is the architecture that suits the target speed and number of bits.

For 8 to 12 bits at low to moderate speed the successive approximation register (SAR) ADC is the usual choice. It finds the digital code by a binary search: starting from the most significant bit (MSB), a comparator decides one bit per clock, so an N-bit conversion needs N comparisons. The converter needs only one comparator, a capacitor DAC and a small controller, and the capacitor DAC draws no static power [1], [6], [8]. In the charge-redistribution form introduced by McCreary and Gray [1], one binary-weighted capacitor array both samples the input and performs the search, so the accuracy depends on capacitor ratios rather than on absolute values. This is why the architecture reaches micro-watt power levels [6], and why it keeps improving through monotonic switching [2] and asynchronous timing with alternate comparators [7].

A SAR ADC also makes a good mixed-signal project, because a sampling switch, a capacitor array, a comparator and a controller all have to work together on a fixed timetable. The sampling switch and the comparator are the critical blocks. A plain MOS switch has an on-resistance that depends on the input signal, which distorts the sample; bootstrapping keeps the gate-source voltage constant and removes this dependence [4]. The comparator must resolve a fraction of an LSB without static power, and the StrongARM latch is a dynamic comparator that does so [3]. The controller must then keep every decision in step with the sampling and output-register events.

Running a full 10-bit converter at transistor level for many conversions is slow, and logic mistakes are hard to find that way. We therefore verify at two levels. Each analog block exists as a transistor-level cell and also as a Verilog-A model [11], so the algorithm and timing can be tested quickly at system level and the transistor-level cells can be checked block by block.

This paper presents a 10-bit SAR ADC designed in Cadence Virtuoso and simulated with Spectre on the 180 nm gpdk180 process. It has a bootstrapped sampling switch, a binary-weighted capacitor DAC from 10 fF to 5.12 pF, a StrongARM latch comparator, a 12-state SAR controller and a 10-bit output register, all driven by one 1 MHz, 5 V clock. A conversion takes 12 clock cycles, which gives 12 µs, 83.3 kS/s and an LSB of 4.883 mV. With a 10 kHz sine input the recorded output matches an ideal quantiser in all 40 conversions, with INL between −0.33 and +0.50 LSB and DNL between −0.42 and +0.39 LSB. Layout, long-record FFT measurement, power measurement and fabrication are outside the scope of this work.

The rest of the paper is organised as follows: Section II reviews related work and states the problem and objectives, Section III describes the tools, architecture and method, Section IV presents the results, applications and cost analysis, and Section V concludes.

2 LITERATURE SURVEY

McCreary and Gray [1] introduced all-MOS charge-redistribution conversion, where one binary-weighted capacitor array both samples the input and carries out the search. Its accuracy depends on capacitor ratios, and the DAC here uses the same structure. Liu et al. [2] built a 10-bit, 50 MS/s SAR ADC with monotonic switching, which cuts the DAC switching energy considerably. Van Elzakker et al. [6] report a 10-bit charge-redistribution ADC that uses 1.9 µW at 1 MS/s, so this architecture can reach micro-watt power. Kull et al. [7] reach 8 bits at 1.2 GS/s with asynchronous timing and alternate comparators; our design keeps a fixed synchronous schedule, which is slower but easier to verify.

Later work concentrated on DAC energy and on speed. Craninckx and Van der Plas [14] reported a 9-bit charge-sharing SAR ADC in 90 nm CMOS that needs 65 fJ per conversion step. Ginsburg and Chandrakasan [15] used a split capacitor array to reduce the DAC capacitance in a 5-bit, 500 MS/s converter in 65 nm, and Hariprasath et al. [16] merged capacitor switching to cut the switching energy further. Zhu et al. [17] built a 10-bit, 100 MS/s SAR ADC in 90 nm that needs no separate reference buffer, and Harpe et al. [18] used asynchronous timing in a 26 µW, 8-bit, 10 MS/s converter for low-energy radios. These designs use advanced nodes and measured silicon, whereas ours is a plain binary-weighted array on an open teaching PDK.

Razavi [3] analyses the StrongARM latch, a dynamic comparator without static power that first appeared in a microprocessor design [19], and we use it. Schinkel et al. [20] added a second tail stage to shorten the decision time of such latches. Abo and Gray [4] keep the gate-source voltage of the sampling switch constant by bootstrapping, which removes the signal-dependent on-resistance. Dessouky and Kaiser [21] applied local bootstrapping to a low-voltage ΔΣ modulator, and Razavi [22] explains the bootstrapped-switch circuit and its limits; our switch follows the same idea. The accuracy of the array depends on matching, and Pelgrom et al. [23] gave the area law for device mismatch. Walden's survey [5] shows how ADC speed and resolution trade off across published designs. Overall, SAR conversion is a proven, ratio-based architecture whose critical blocks are the sampling switch and the comparator. Few papers, though, show

a clear path from Verilog-A models down to transistor-level cells on an open teaching PDK, and that is the gap this work fills.

2.1 Problem Statement

A full transistor-level simulation of a 10-bit SAR ADC takes a long time. A plain MOS sampling switch has an on-resistance that depends on the signal and so distorts the sample. The comparator has to resolve a fraction of an LSB without static power, and the controller has to stay in step with the sampling and output-register events. What is needed is a documented design that (i) samples through a switch whose on-resistance does not depend on the input, (ii) uses a 10-bit binary-weighted capacitor DAC, (iii) makes one dynamic comparison per clock, (iv) completes ten bit trials per conversion and loads an output register, and (v) is verified at behavioural and transistor level on gpdk180.

3 METHODOLOGY

3.1 Tool and Technology Platform

Design and simulation were done in Cadence Virtuoso with the Analog Design Environment and Spectre, using the gpdk180 kit and the analogLib library [12]. The behavioural models are written in Verilog-A [11] and all follow one pattern. Input voltages are compared with a threshold v_{trans} = 2.5 V, state is kept in real variables that update at clock events @(cross(V(clk)−2.5,+1)), and outputs are driven by V(out) + transition(value, delay, ttime) with a 1 ps edge. This lets a discrete-time algorithm run together with analog circuits in a single Spectre simulation.

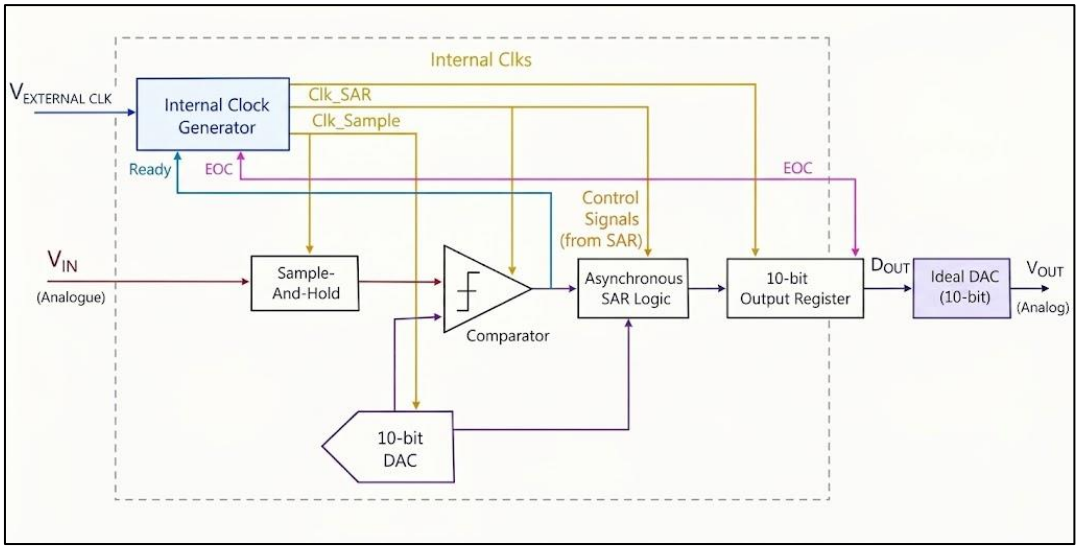


Figure 1: Top-level architecture of the 10-bit SAR ADC.

3.2 Overall data flow

The sampling clock closes the bootstrapped switch, and the input is stored on a capacitor (Fig. 1). The SAR controller then puts a 10-bit trial word on the capacitor DAC, MSB first. The StrongARM comparator gives one decision per clock, and the controller keeps or clears the trial bit and sets the next one. After D0 is decided, a register clock loads D9–D0 into the output register. Every block uses the same clock. With reference V_{REF} and N bits, the LSB is

$$V_{LSB} = \frac{V_{REF}}{2^N} = \frac{5\ V}{1024} \approx 4.883\ mV \quad (1)$$

3.3 Bootstrapped sampling switch

The on-resistance of an NMOS switch depends on its gate-source voltage, which follows the input [9], [10]:

$$R_{on} \approx \frac{1}{\mu_n C_{ox}\left(\frac{W}{L}\right)(V_{GS}-V_{th})} \quad (2)$$

The 1.4 pF bootstrap capacitor is charged to the supply while the switch is off. During sampling it is connected between source and gate, so $V_{GS} \approx V_{DD}$ whatever V_{in} is, and R_{on} stays nearly constant [4]. This removes the main source of sampling distortion. Charge injection and clock feedthrough remain, and only careful sizing or dummy devices reduce them. The thermal noise sampled on a total capacitance C_T is

$$v_{n,rms} = \sqrt{\frac{kT}{C_T}} \qquad (3)$$

3.4 Charge-redistribution capacitive DAC

The DAC is a binary-weighted array with a unit capacitor C_u = 10 fF. Fig. 2 shows the fully differential 10-bit circuit. Each side has ten binary-weighted capacitors from 512C down to C, a unit dummy capacitor, a bootstrapped input switch, a reset switch to V_{CM}, and bottom-plate switches that connect each capacitor to the input or to a reference rail according to D_i. The capacitor values are

$$C_i = 2^i C_u, \quad C_T = \sum_{i=0}^{N-1} C_i = (2^N - 1)C_u \qquad (4)$$

giving 10, 20, 40, 80, 160, 320, 640 fF, 1.28, 2.56 and 5.12 pF, which add up to 10.23 pF (the dummy capacitor is not counted). During conversion each bottom plate goes to V_{REF} (bit = 1) or to ground (bit = 0). By charge conservation, for an ideal array with a unit dummy capacitor,

$$V_x = -V_{in} + V_{REF} \sum_{i=0}^{N-1} b_i 2^{i-N} \qquad (5)$$

so the top plate reaches the comparator threshold exactly when the DAC word equals the input. The Verilog-A model uses

$$V_{DAC} = V_{min} + \frac{V_{max} - V_{min}}{2^N} \sum_{i=0}^{N-1} b_i 2^i \qquad (6)$$

The DAC works in three phases. In the sampling phase the bottom plates are tied to V_{in} and the top plate is held at V_{cm}. In the hold phase the top plate is isolated and the input charge stays on the array. In the redistribution phase the controller applies the trial words. Each trial must settle to within half an LSB before the comparator fires, so for a first-order time constant $R_{on}C_T$ we need

$$t_s \geq (N+1) \ln 2 R_{on} C_T \qquad (7)$$

Half of the 1 µs clock period (500 ns) is available, and with C_T = 10.23 pF the switch resistance must stay below about 6.4 kΩ. The main non-idealities of the array are capacitor mismatch and top-plate parasitics. Mismatch in the large capacitors would show up as DNL errors at the major code transitions. A parasitic capacitance C_p on the top plate scales each DAC step by $C_T/(C_T+C_p)$, so both have to be kept small in layout.

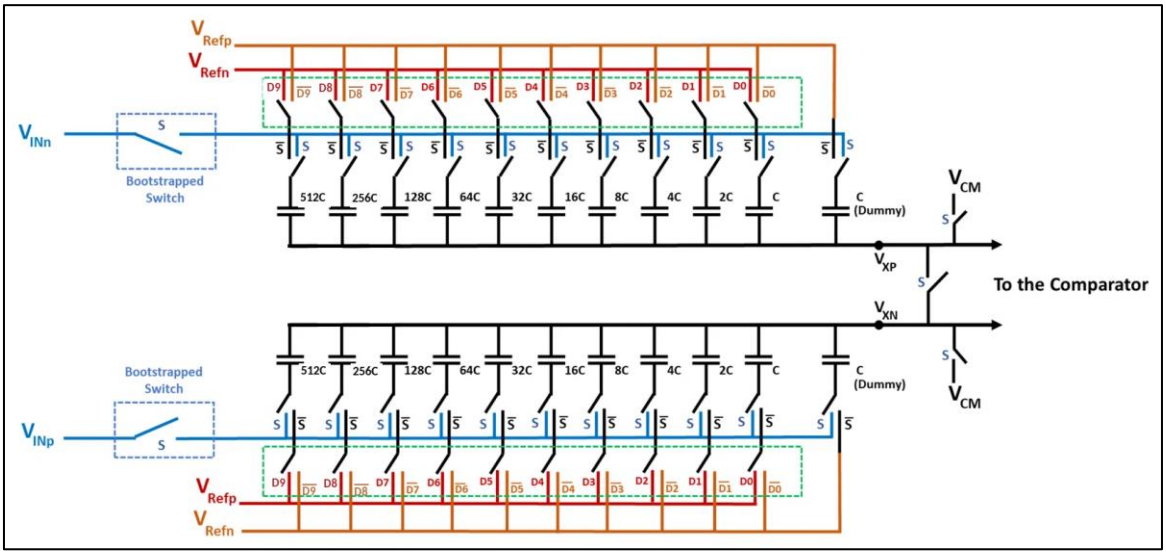


Figure 2: Fully differential 10-bit charge-redistribution DAC with bootstrapped input switches.

3.5 StrongARM latch comparator

The StrongARM latch [3] precharges while the clock is low and uses no static current. When the clock rises, the input pair unbalances the two branches and a cross-coupled pair regenerates the difference to full logic levels. At 1 MHz there are 500 ns per decision, which is a wide margin. The system model gives V_{dout} = 5 V if $V_{in} \geq V_{ref}$ and 0 V otherwise. In a real latch the input-referred offset adds to the decision threshold and must stay below half an LSB (2.44 mV) to avoid

code errors, and regeneration kicks charge back into the DAC. The input pair is therefore the device to size carefully, and offset calibration would be a natural extension.

3.6 SAR algorithm and controller

For bit k, from N−1 down to 0, the trial voltage and decision are

$$V_{trial,k} = V_{REF}\left[\sum_{j=k+1}^{N-1} b_j 2^{j-N} + 2^{k-N}\right] \qquad (8)$$

$$b_k = 1 \text{ if } V_{in} \geq V_{trial,k};\ \ b_k = 0 \text{ otherwise} \qquad (9)$$

A counter sar_counter runs from 11 to 0 (Fig. 3). State 11 clears the word and asserts the sampling enable. State 10 applies the MSB trial. States 9 to 1 each resolve the previous bit and apply the next. State 0 resolves D0 and returns to 11, where the register clock is asserted on the falling edge. Fig. 4 shows the transistor-level circuit for 10 bits. A sequencer of twelve TSPC D flip-flops (N + 2, one per state) is clocked by clk_sar. On reset the first flip-flop is set and the others are cleared, so one token moves along the chain; the last stage feeds back to the first and also gives the end-of-conversion signal EOC. Stages 2 to 11 each set one flip-flop of the code register, D[9] down to D[0], which applies that bit as the trial value. Each code flip-flop takes Comparator_out at its D input and is clocked by the next lower bit, so it stores the decision just as the next trial bit is applied. A dummy flip-flop with its D input tied low is set by EOC, and its rising output clocks D[0]. The TSPC flip-flop used everywhere is drawn at the bottom of the figure; its set and reset transistors (brown) force a known state at the start of each conversion.

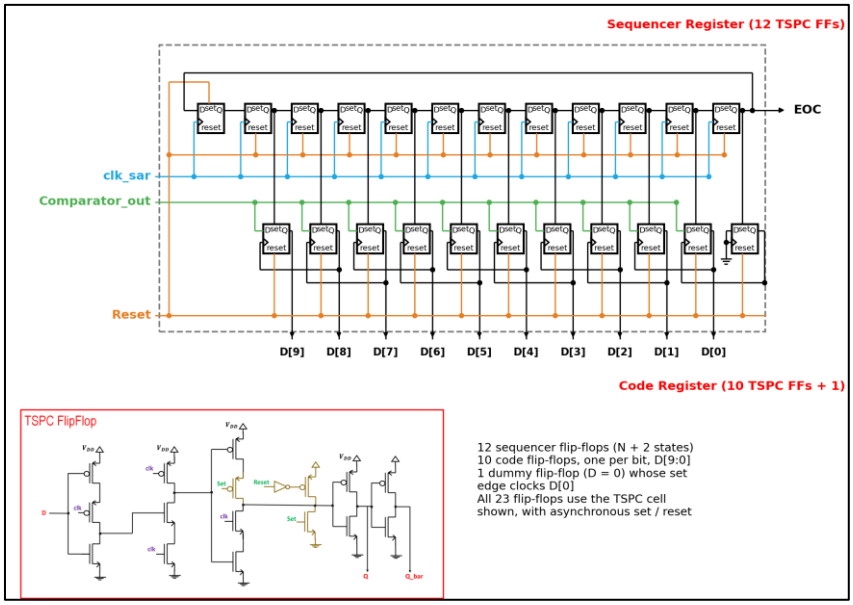


Figure 3: Transistor-level 10-bit SAR logic: a 12-stage sequencer register and a 10-bit code register built from TSPC D flip-flops with set/reset

3.7 Timing and output register

One sample/reset cycle, ten bit trials and one register cycle give

$$T_{conv} = (N+2)T_{clk},\ \ f_s = \frac{f_{clk}}{N+2} \approx 83.3\ \text{kS/s} \qquad (10)$$

The output register copies D9–D0 on the register clock and holds them for a full conversion, so the output shows up one conversion period (12 µs) after the sampling instant. The library also has a 1 ns delay cell, XOR, AND, inverter and 2:1 MUX for clock generation.

3.8 Implementation Methodology

The work had five phases. Each transistor-level cell was first drawn in gpdk180 and tested with analogLib sources. Every block was then rewritten in Verilog-A with a 5 V logic convention. The controller, comparator, DAC, sample-and-hold and register were wired into a top-level SAR_ADC schematic and test bench. For verification, the controller was tested alone with an alternating comparator input, and then the full converter with a 10 kHz sine. Finally, the waveforms

were read with cursors and compared with Sections III-B to III-G, and the parameters of Table IV were extracted from the output record (Sections IV-G and IV-H).

4 RESULTS AND ANALYSIS

4.1 Test set-up

The input is $v_{in}(t) = 2.5\ V + 0.1\ V \cdot \sin(2\pi \cdot 10\ kHz \cdot t)$, the clock is 1 MHz, and 500 µs is simulated (41 conversions, five input periods). The parameters are listed in Table I.

Table 1: Design and test parameters

Parameter	Value
Resolution / technology	10 bit / gpdk180
Logic level / full scale	5 V / 5 V
LSB	4.883 mV
Unit cap. / total array	10 fF / 10.23 pF
Clock frequency	1 MHz
Cycles per conversion	12 (1 + 10 + 1)
Conversion time / sample rate	12 µs / 83.3 kS/s
Output latency	1 conversion (12 µs)

4.2 Controller and register verification

Fig. 5 shows the controller on its own. After reset D9 is set as the first trial. The comparator result is 0, so D9 is cleared and D8 is set. One bit is resolved per clock down to D0 (markers V1–V10), as in Fig. 3. For this stimulus the final word is 0101010101 (341). The register clock goes high after the twelfth cycle, at about 165–180 µs, which matches 12 × 15 µs = 180 µs. When this word is fed in, the output register changes all ten outputs together at the register clock and then holds them, so a downstream reader never sees a half-updated code.

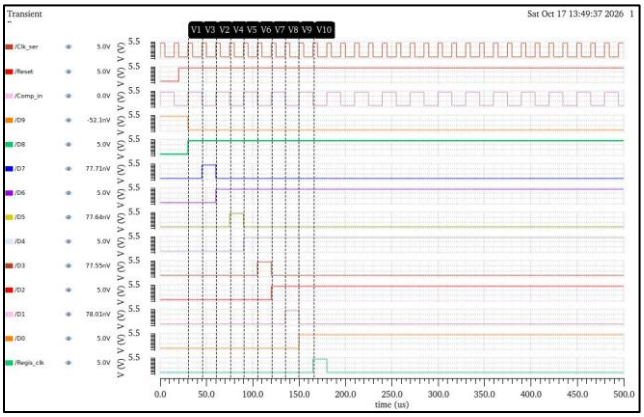


Figure 4: Transient verification of the SAR controller with an alternating comparator input (markers V1–V10, 15 µs apart).

4.3 Complete converter

Fig. 6 shows the full converter. Sampling and register-clock pulses appear every 12 µs, which confirms the 12-cycle schedule and the 83.3 kS/s rate. The sampled input is a staircase that follows the sine, and the reconstructed output tracks it with a delay over five periods, with no missing or repeated conversions. The input sampled at 12 µs and 24 µs is 2.568 V and 2.598 V, and the recorded output reaches 2.568 V and 2.598 V one conversion later, which confirms the 12 µs latency from Section III-G.

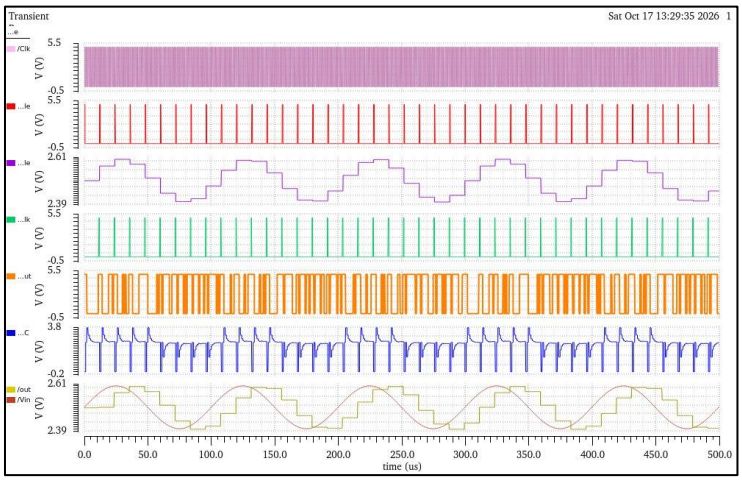


Figure 5: Complete ADC over 500 µs with a 10 kHz sine input: clocks, sampled input, comparator output, DAC-side node and reconstructed output (bottom).

4.4 Quantisation and noise

For a sine of amplitude A in a full-scale range V_{FS}, the ideal quantisation-limited SQNR is

$$\mathrm{SQNR} = 6.02N + 1.76 + 20\log_{10}\left(\frac{2A}{V_{FS}}\right)\ \mathrm{dB} \quad (11)$$

For N = 10 this gives 61.96 dB at full scale. The test input covers only $2A/V_{LSB}$ = 41 codes, so its ideal SQNR is 34.0 dB; it was chosen to show tracking and timing, not to use the full range. With C_T = 10.23 pF at 300 K, (3) gives $v_{n,rms}$ = 20.1 µV, only 0.4% of an LSB, so the array size is set by matching and not by noise. The effective resolution follows from the signal-to-noise-and-distortion ratio (SNDR) as

$$\mathrm{ENOB} = \frac{\mathrm{SNDR} - 1.76}{6.02} \quad (12)$$

so the 34.0 dB ideal SQNR of the test input corresponds to about 5.4 bits for its 41 codes, against the 10-bit full-scale limit. The SNR measured from the output record (Section IV-H) is 33.7 dB, close to this value.

4.5 Error sources

Four effects would limit a real implementation. (i) Comparator offset must stay below half an LSB, 2.44 mV, or the decision threshold moves by more than a quantisation step. (ii) Capacitor mismatch causes DNL errors, largest where the 5.12 pF and 2.56 pF capacitors switch. (iii) Charge injection and clock feedthrough from the sampling switch add a signal-dependent error to the held sample. (iv) Incomplete DAC settling breaks the bound in Section III-D. Thermal noise at 20.1 µV rms is negligible. Offset, injection and settling would be quantified by the Monte Carlo and post-layout analyses planned in Section V.

4.6 INL and DNL

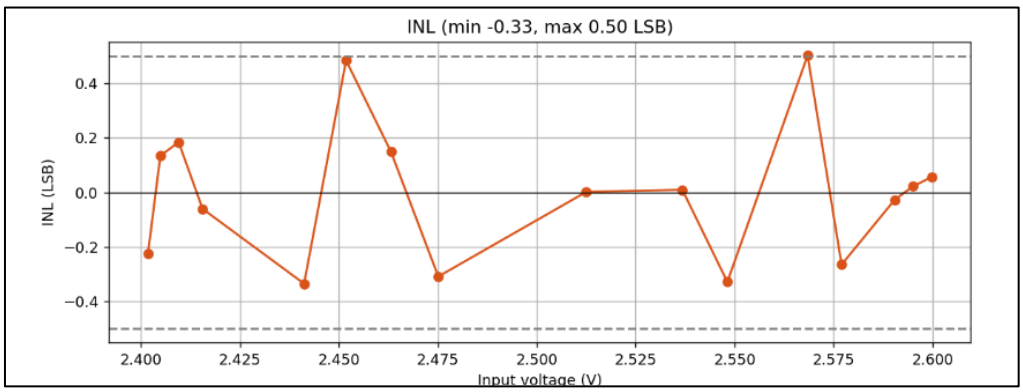


Figure 6: INL versus input voltage (min −0.33 LSB, max 0.50 LSB).

INL and DNL were taken from the simulated output record (ADC.csv) with repeated output values removed. Fig. 7 shows the INL against input voltage and Fig. 8 shows the DNL against sample number. Table III lists the values read from the two plots (about ±0.01 LSB reading accuracy); the sample number is the rank of the point in increasing input voltage, and DNL starts at sample 2 because it is a difference between neighbouring levels.

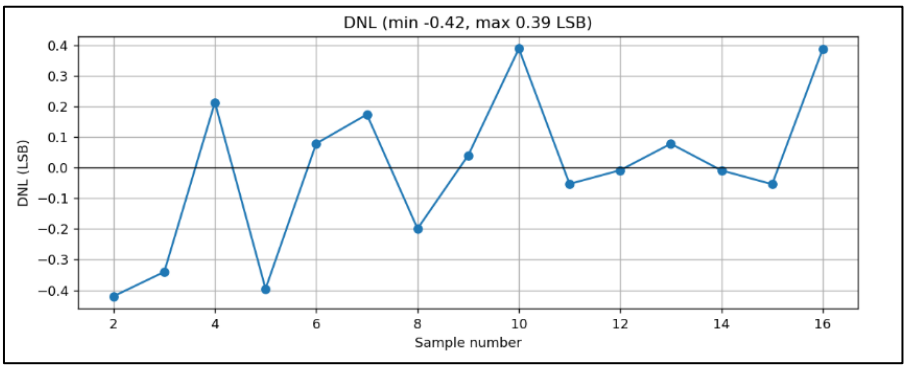


Figure 7: DNL versus sample number (min −0.42 LSB, max 0.39 LSB).

Table 2: INL and DNL read from Figs. 7 and 8

Sample	Vin (V)	INL (LSB)	DNL (LSB)
1	2.402	−0.23	–
2	2.405	+0.13	−0.42
3	2.409	+0.18	−0.34
4	2.415	−0.06	+0.21
5	2.441	−0.33	−0.39
6	2.452	+0.48	+0.08
7	2.463	+0.15	+0.18
8	2.475	−0.31	−0.20
9	2.512	0.00	+0.04
10	2.537	+0.01	+0.39
11	2.548	−0.33	−0.05
12	2.568	+0.50	−0.01
13	2.577	−0.26	+0.08
14	2.591	−0.03	−0.01
15	2.595	+0.02	−0.05
16	2.600	+0.05	+0.39

The INL stays between −0.33 and +0.50 LSB and the DNL between −0.42 and +0.39 LSB. The DNL never reaches −1 LSB, so no code is missing in the record. The 10 kHz test sine only visits codes 491 to 532, so these values describe that part of the transfer curve and not the whole range.

4.7 Parameters from the output record

The parameters in Table IV were calculated from ADC.csv using one value per 12 µs conversion, so the repeated points inside each conversion are not counted. With the input taken as 2.5 V + 0.1 V·sin(2π·10 kHz·t), the recorded output equals the floor of v_{in}/V_{LSB} in all 40 conversions, that is, it matches an ideal 10-bit quantiser delayed by one conversion. The quantisation error is the output code minus the input in LSB plus 0.5. The SNR is the rms of the 0.1 V input divided by the rms quantisation error, and the ENOB is (SNR − 1.76 + 20 $\log_{10}(V_{FS}/2A)$)/6.02. The dynamic range is the rms of a full-scale sine divided by the same error. The gain error is the slope of output code against input code, minus one, from

a straight-line fit. The sampling rate follows from the 12 µs spacing of the output updates. The record is short, so the gain error is only known to about ±0.3%.

Table 3: Parameters extracted from the output record

Parameter	Value
Gain error	+0.66% (±0.31%)
Quantisation error	0.30 LSB rms, 0.50 LSB peak
Missing codes	None (DNL > −1 LSB)
Monotonicity	Monotonic
SNR	33.7 dB
Dynamic range	61.7 dB
DNL	−0.42 / +0.39 LSB
INL	−0.33 / +0.50 LSB
ENOB	9.95 bits
Sampling rate	83.3 kS/s

5 CONCLUSION AND FUTURE SCOPE

This paper presented a 10-bit SAR ADC in gpdk180 with a bootstrapped sampling switch, a 10 fF–5.12 pF binary-weighted capacitor DAC, a StrongARM latch, a 12-state controller and an output register, together with a matching Verilog-A library. A conversion takes 12 cycles (12 µs at 1 MHz, 83.3 kS/s, 4.883 mV LSB). Simulation showed ordered bit resolution, an atomic register update, and tracking of a 10 kHz sine with one conversion of latency. From the output record, INL lies between −0.33 and +0.50 LSB, DNL between −0.42 and +0.39 LSB with no missing codes, and the SNR is 33.7 dB, which gives an ENOB of 9.95 bits. Future work includes layout and post-layout simulation, Monte Carlo mismatch analysis with real process data, full-range INL/DNL and FFT measurement following IEEE Std 1241 [13], monotonic switching [2], asynchronous clocking [7], offset calibration and an FPGA interface.

STATEMENTS ON COMPLIANCE WITH ETHICAL STANDARDS

Disclosure of conflict of interest

The authors declare no conflicts of interest regarding this manuscript.

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